# Metal contamination in process line of superconducting quantum processor chips*

XU Xiao[1], ZHANG Haibin[2,*], SU Feifan[2,3,*], YAN Kai[2], RONG Hao[3], DENG Hui[2,3], YANG Xinying[1], MA Xiaoteng[1], DONG Xue[1], WANG Qiming[1], LIU Jialin[1], LI Manman[1]

1. Jinan Institute of Quantum Technology, Jinan 250101, China
2. Hefei National Laboratory, Quantum Computing Department, Hefei 230094, China
3. University of Science and Technology of China, CAS Center for Excellence in Quantum Information and Quantum Physics, Hefei 230026, China

**Abstract**

The manufacturing process of superconducting quantum processor chips faces special challenges of metal contamination, and their material system and process characteristics are significantly different from those of traditional semiconductor chips. This study focuses on the issue of metal contamination in the fabrication process of quantum chips, systematically analyzing the sources, diffusion mechanisms, and prevention strategies of metal contamination in quantum chips, where the bulk diffusion and surface diffusion behaviors of superconducting materials (such as Ta, Nb, Al, TiN) on sapphire and silicon substrates are particularly emphasized.

The results show that the sapphire substrate, due to its dense lattice structure, exhibits excellent anti-diffusion performance, reducing the risk of contamination and providing a stable interface environment for superconducting quantum chips. For silicon substrates, special attention must be paid to the contamination risks from high-mobility metals such as Au, In, and Sn. Experimental verification shows that Ti/Au under bump metallization structures on silicon substrates are prone to Au penetration diffusion, and increasing Ti thickness does not significantly improve the blocking effect. The low-temperature process (< 250 ℃) and ultra-low-temperature operating environment (mK level) of quantum chips effectively suppress metal

* The paper is an English translated version of the original Chinese paper published in Acta Physica Sinica. Please cite the paper as: XU Xiao[1], ZHANG Haibin[2,*], SU Feifan[2,3,*], YAN Kai[2], RONG Hao[3], DENG Hui[2,3], YANG Xinying[1], MA Xiaoteng[1], DONG Xue[1], WANG Qiming[1], LIU Jialin[1], LI Manman[1], **Metal contamination in process line of superconducting quantum processor chips**. *Acta Phys. Sin.*, 2026, 75(1):010601. doi: 10.7498/aps.75.20251101

diffusion, but the exposed metal surfaces and material diversity still pose unique challenges.

The study recommends establishing a dedicated metal contamination prevention system for quantum chips and proposes future research directions, including the evaluations of novel materials, surface state regulation, and long-term reliability studies. This work provides important theoretical support and technical guidance for optimizing the process and enhancing the performance of superconducting quantum chips.

**Keywords:** superconducting quantum processor chip; process-line metallic contamination; bulk diffusion; surface diffusion;
**PACS:** 85.40.-e; 85.40.Ls; 68.35.Md; 68.35.Fx
**DOI:** 10.7498/aps.75.20251101
CSTR: 32037.14.aps.75.20251101

# 1 Introduction

The two major theoretical breakthroughs in 20th-century physics-quantum science and relativity-laid a crucial foundation for modern technological advancement. In recent years, the practical implementation of quantum technologies has accelerated significantly. Among these, superconducting quantum computing has emerged as one of the most promising technical pathways, owing to its ability to directly leverage mature semiconductor industry experience and its potential for scalable expansion. After decades of development, the semiconductor industry has established a modernized process system primarily centered around 12-inch wafers. This industrial ecosystem originated in the post-World War II era and, through prolonged development, not only cultivated a vast pool of specialized talent but also built a comprehensive industrial chain encompassing standards, regulations, and system frameworks. Notably, the industry has demonstrated sustained innovation and rapid iteration capabilities based on "Moore's Law," particularly in semiconductor materials, production equipment, and manufacturing processes, providing crucial support for the advancement of quantum computing technology.

Competition in quantum computing has intensified globally. In December 2024, Google released its quantum processor "Willow: Quantum for AI," achieving a major breakthrough in quantum error correction[1]. In March 2025, China unveiled the "Zuchongzhi-3" superconducting quantum computer, whose core metric of 105 qubits and multiple key performance indicators surpassed those of Google's Willow chip, though it lagged slightly in error correction capability[2]. This milestone signifies China's entry into the global forefront of superconducting quantum computing.

Nevertheless, compared with international leaders, China still faces gaps in industrial-scale fabrication processes. For instance, Belgium's Interuniversity Microelectronics Centre (IMEC) has already achieved large-scale production of superconducting qubits on a 300 mm complementary metal-oxide-semiconductor (CMOS) line, attaining a wafer yield of 98.25%[3]. In contrast, China's "Zuchongzhi-3" still relies on a laboratory-scale 3-inch process line, indicating a need for further enhancement in process maturity and industrialization capacity.

In light of this situation, this study focuses on metal contamination in quantum chip fabrication processes, systematically investigating its underlying mechanisms to provide theoretical foundations and technical references for process optimization and to accelerate the industrialization of China's quantum computing technologies. Current quantum computing research remains in the fundamental stage, with numerous scientific and engineering challenges requiring sustained collaborative innovation between academia and industry.

# 2 Analysis and Discussion

Metal contamination, a long-standing issue in semiconductor chip manufacturing, poses severe challenges to device performance and reliability. Quantum chip fabrication largely adopts established semiconductor technology pathways. Therefore, before systematically examining metal contamination effects in quantum chips, it is essential to first investigate the sources, migration mechanisms, and impacts on electrical characteristics of metal contamination in conventional semiconductor devices. This approach not only helps establish a cognitively coherent framework rooted in technological continuity but also offers targeted insights for the unique process requirements of quantum chips.

## 2.1 Metal Contamination Control in Semiconductor Chips

### 2.1.1 Origins of Metal Contamination in Semiconductor Chips

Metal contamination arises primarily from two sources: (1) intentional metal thin-film materials used in fabrication processes and (2) unintended metallic impurity atoms introduced from external environments or process steps. These contaminants adversely affect semiconductor devices because metals exhibit high diffusion coefficients in silicon, introduce deep-level defects within the bandgap, reduce carrier lifetimes, and significantly degrade electrical performance-such as increasing leakage current and shifting threshold voltage[4].

Semiconductor chips are especially sensitive to transition metals (e.g., Fe, Cu, Ni, Co), alkali metals (e.g., Na, K), and heavy metals (e.g., Au, Ag). Copper diffuses rapidly in

silicon, and iron is one of the most common sources of contaminants, significantly reducing the lifetime of minority carriers and increasing leakage current.

### 2.1.2 The Latency and Severe Consequences of Metal Contamination

Metal contamination in semiconductor manufacturing exhibits three hallmark characteristics: strong latency, pronounced diffusion effects, and systemic risk. Its latency manifests as an absence of early symptoms; conventional detection methods often fail to identify contamination during initial stages, with performance degradation typically emerging only during device operation. Even trace amounts of metallic impurities (at ppb levels) can severely impair device functionality. The diffusion effect is particularly significant for transition metals (e.g., Fe, Cu, Ni), which possess high diffusion coefficients in silicon and primarily migrate via interstitial diffusion and high-temperature dissolution under thermal equilibrium[5]. High-temperature processes in chip fabrication-such as annealing and oxidation-accelerate this diffusion. Furthermore, metal contamination poses systemic risks, as it can spread cross-contamination through equipment, carriers, and gas lines, rapidly propagating across multiple process tools and potentially forcing entire production lines into shutdown for maintenance. Decontamination is both costly and often ineffective.

Under the semiconductor industry's current "winner-takes-all" competitive landscape, a single severe contamination incident can cause a company to lose its technological leadership. Consequently, establishing a robust preventive monitoring system and rapid response mechanism constitutes an indispensable quality assurance measure in advanced semiconductor manufacturing.

### 2.1.3 Metal Contamination Control Framework in Semiconductor Manufacturing

The metal contamination control system in semiconductor chip fabrication is a multi-layered, end-to-end precision control framework, comprising the following core measures[6]. In material source control, ultra-high-purity materials are employed: silicon wafers (≥99.9999999% purity), chemical reagents (SEMI Grade C12 or higher), and electronic-grade gases (e.g., $NF_3$). Gettering techniques-such as hydrogen annealing-are applied to wafers to trap metallic impurities (e.g., Fe, Cu) via lattice defects and optimize substrate quality. For process environment control, cleanroom standards require Class 1-10 (ISO Class 3-4) environments to manage particulate and metallic aerosol levels. Equipment passivation involves coating reaction chambers and pipeline interiors with corrosion-resistant layers (e.g., quartz, SiC) to minimize metal flaking. Dedicated tools are physically segregated-for example, copper-process

equipment is isolated from aluminum-process equipment to prevent cross-contamination. In process-level contamination control, low-temperature processing is adopted to suppress metal diffusion at elevated temperatures (e.g., backend interconnect processes maintained at ≤400 °C); diffusion barrier layers (Figure 1) such as TaN/TiN are embedded within dielectric layers; and silicide contact layers (e.g., NiSi) are used to inhibit metal penetration. Cleaning protocols employ RCA standard cleans (SC1/SC2) to remove surface metals, while dilute hydrofluoric acid (DHF) strips the native oxide layer along with adsorbed metallic contaminants.

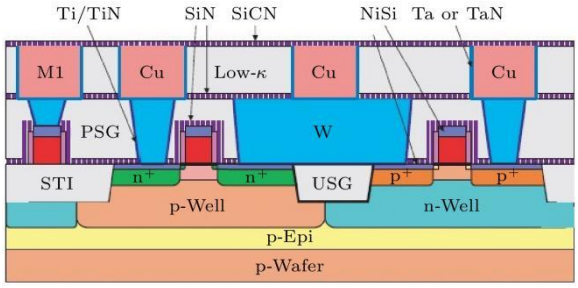


**Fig. 1 Schematic diagram of TaN/TiN diffusion barrier layers and NiSi contact layer in semiconductor chips[7].**

## 2.2 Differences Between Semiconductor Chips and Quantum Chips

In the initial phase of establishing a fabrication line for superconducting quantum processor chips, the research team acutely recognized fundamental differences between quantum processor chips and conventional semiconductor chips. The quantum domain cannot directly adopt the mature methodologies of the semiconductor industry. Key parameters of semiconductor devices-such as the maximum operating frequency ($F_{max}$) and static leakage currents ($I_{DD\ quiescent}$, $I_{DDQ}$) of logic communication chips-have well-established and clearly elucidated relationships with CMOS device parameters. Their influencing factors are relatively well-defined, and the underlying mechanisms are thoroughly understood.

In contrast, critical performance metrics of quantum chips-including qubit energy relaxation time ($T_1$), pure dephasing time ($T_\varphi$), intrinsic resonator quality factor ($Q_i$), and external quality factor ($Q_e$)-are subject to complex, coupled influences from design, materials, fabrication processes, and measurement systems. Moreover, the interrelationships among these factors remain incompletely understood. This complexity renders current quantum chip fabrication processes effectively a "black box," wherein many critical process parameters cannot be precisely defined or quantified, posing significant challenges to process optimization and performance enhancement.

Table 1 briefly summarizes the primary differences between semiconductor chips and

superconducting quantum chips in terms of device architecture, material selection, process characteristics, and operating environments.

**Table 1** Comparison of process characteristics between conventional semiconductor chips and superconducting quantum chips.

| | | Semiconductor chip | Superconducting quantum chip |
|---|---|---|---|
| Device | | CMOS field-effect transistors | Transmon structure of the Josephson junction |
| Material | Substrate | Si, InP, SiC | Sapphire, high-resistance silicon |
| | FEOL | Semiconductor doping | Superconducting metals, dielectric materials |
| Technology | | Ion implantation, thermal processing | Organic cleaning , stripping |
| Environment | Temperature | –40—150 ℃ | mK-level low temperature |
| | Humidity | Standard environment: 30%–70% relative humidity (RH) or a broader range | Vacuum environment |
| | Electromagnetism | General environment (except for special scenarios such as space applications) | Electromagnetic shielding |

## 2.3 Specific Characteristics of Metallic Contamination in Quantum Chips

Based on differences in material systems and process characteristics between semiconductor and quantum chips, quantum chip fabrication exhibits several distinctive features regarding metallic contamination control. Device components directly employ superconducting metals, precluding front-end and back-end isolation as practiced in semiconductor chip manufacturing. Air gaps rather than dielectric layers are used for isolation, resulting in persistent surface diffusion pathways for metal atoms. As illustrated in Figure 2, the aluminum crossover bridges interconnecting the ground planes of coplanar waveguide (CPW) transmission lines pose a specific risk: if aluminum atoms from these bridges diffuse across the silicon dioxide surface and reach the CPW signal line, they can form a conductive path between the bridge and the ground plane, directly causing a short circuit in the coplanar waveguide. The use of high-temperature processes is restricted, thereby suppressing both bulk and surface diffusion of metal atoms. Because exposed metallic structures exist on the surface, conventional semiconductor acid-cleaning procedures

cannot be directly applied to remove surface metal atoms, limiting the broad applicability of this method. The substrate primarily serves a mechanical support function and does not participate in device formation, rendering it less susceptible to metal diffusion effects. Additionally, the operating current remains low (on the order of μA), reducing the risk of electric-field-induced diffusion.

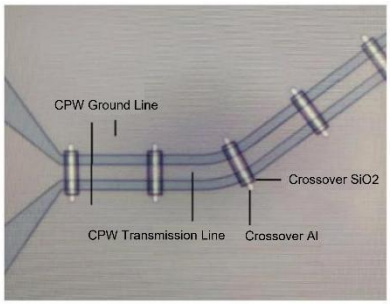


**Fig. 2 Aluminum crossover bridge structure for CPW transmission line and ground interconnects in quantum chips.**

## 2.4 Diffusion Characteristics of Metallic Materials in Quantum Chips

Currently, in-depth research on metallic contamination in quantum chips remains in its infancy both domestically and internationally, with extremely limited experimental data and theoretical foundations. Compared to the well-established understanding of metallic contamination in conventional semiconductor chips, the mechanisms and impacts of metallic contamination in quantum chips have not yet formed a systematic conceptual framework. In light of this gap, this study first focuses on two fundamental failure modes induced by metallic contamination: circuit shorting and leakage current. These issues primarily arise from bulk diffusion of metallic impurities through dielectric layers and surface diffusion on sample substrates. The investigation selects representative superconducting materials widely used in quantum chips-including both device and interconnect materials-such as Ta, Nb, Al, TiN, In, and Sn, with particular emphasis on their diffusion characteristics. Additionally, considering practical fabrication constraints, certain non-superconducting metals (e.g., Ti, Au) may still be employed as interconnect materials; thus, these are also included in the study to comprehensively evaluate the potential impacts of diverse metallic systems on quantum chip performance. This focused research framework aims to establish foundational experimental data and theoretical insights into metallic contamination in quantum chips, thereby providing essential technical support for subsequent mechanistic investigations.

### 2.4.1 Bulk Diffusion of Metallic Materials in Quantum Chips

Bulk diffusion refers to atomic migration through the interior of a crystal lattice, typically requiring elevated temperatures for activation. It correlates with a material's melting point, crystal structure, and defect density[8,9].

1) Diffusion in silicon (Si). Refractory metals (Ta, Nb, Ti) and their nitrides (TiN) exhibit extremely low diffusion coefficients in Si, showing significant diffusion only at high temperatures (>800 ℃) via a vacancy-mediated mechanism. These metals react with Si to form silicides (e.g., $NbSi_2$, $Ta_2Si$), substantially altering diffusion pathways[10]. TiN shows negligible diffusion in Si and is therefore commonly used as a diffusion barrier[11]. In contrast, the fast-diffusing element Au exhibits very high diffusivity in Si (even at 300-400 ℃), readily penetrating Si through grain boundaries or defects and degrading device performance[12,13]. Al diffuses moderately in Si (requiring 500-600 ℃) and is frequently used for doping. In and Sn diffuse rapidly due to their low melting points, with Sn particularly prone to silicide formation at elevated temperatures.

2) Diffusion in silicon dioxide ($SiO_2$). As an insulating layer, $SiO_2$ effectively blocks diffusion of refractory metals (Ta, Nb, Ti); TiN is commonly employed as a barrier layer between Cu/$SiO_2$. Au diffuses slowly in $SiO_2$ and shows limited chemical interaction[14], though it may still permeate through defects at high temperatures. Al diffuses slowly in $SiO_2$ (requiring high temperatures), while In and Sn, owing to their low melting points, tend to accumulate at interfaces.

3) Diffusion in sapphire ($Al_2O_3$)[15]. Sapphire is a dense single crystal with high diffusion energy barriers, resulting in extremely slow diffusion for most metals (except Au). Au may diffuse along surface defects, whereas Al exhibits low diffusivity due to elemental compatibility with the substrate.

### 2.4.2 Surface Diffusion of Metallic Materials Used in Quantum Chips

Surface diffusion is influenced by atomic adsorption energy, substrate surface energy, and temperature, with low-melting-point metals exhibiting greater mobility.

1) On silicon (Si) surfaces. Metals such as Au, Al, In, and Sn, which have low melting points, readily migrate and tend to form islands or droplets (e.g., In/Sn agglomeration into spheres at elevated temperatures). Au readily forms silicides on Si surfaces and exhibits low-temperature eutectic behavior (e.g., AuSi eutectic point at ~363 ℃)[16]. Ti and TiN show low surface mobility and tend to form uniform coatings; TiN is commonly used as an adhesion layer.

2) On silicon dioxide ($SiO_2$) surfaces. Au has high surface energy and tends to agglomerate on $SiO_2$; Cr/Ti adhesion layers are often required to improve its

wettability. Al demonstrates good wettability on $SiO_2$, whereas In/Sn readily form nanoparticles[17].

3) On sapphire ($Al_2O_3$) surfaces. The high surface energy promotes metal agglomeration (e.g., Au spheroidization). Ti/TiN enhance film uniformity due to strong interfacial bonding.

### 2.4.3 Key Influencing Factors

The diffusion and migration rates of metals are affected by temperature, interfacial reactions, and defects or grain boundaries. Elevated temperatures significantly accelerate diffusion and migration (e.g., Sn begins to flow above 200 ℃). Interfacial reactions can promote metal diffusion and migration-for instance, Ti/Si forms silicides, Au/Si forms eutectics, and Al/$SiO_2$ may reduce the oxide. Defects and grain boundaries enhance metal diffusion, as observed in polycrystalline substrates (e.g., polycrystalline $SiO_2$), where diffusion occurs more rapidly.

### 2.4.4 Comparison Between Bulk and Surface Diffusion

Table 2 compares the characteristics of bulk diffusion ($D_{bulk}$) and surface diffusion ($D_s$). Surface diffusion is characterized by low activation energy and high mobility, rendering surface processes typically faster than bulk processes.

**Table 2** Comparison of physical characteristics between metal bulk diffusion and surface diffusion[18].

| Characteristics | Bulk diffusion | Surface diffusion |
|---|---|---|
| Activation energy | Higher (1–5 eV) | Lower (0.1–2.0 eV) |
| Temperature-dependent | Sensitive | More sensitive (exponential relationship) |
| Dominant Mechanism | Vacant space，gap | Jump， Exchange |
| Typical Rate | Slow | Faster (Ds≫Dbulk) |

## 2.5 Comprehensive Analysis of Diffusion Characteristics and Contamination Control of Metallic Materials in Quantum Chips

### 2.5.1 Diffusion Characteristics of Metallic Materials in Quantum Chips

Different substrates and metallic materials exhibit significant variations in diffusion behavior during quantum chip fabrication, directly affecting device performance and reliability. Sapphire ($Al_2O_3$) demonstrates excellent resistance to metal diffusion due to its dense crystal lattice and exceptional chemical stability (melting point of 2050 ℃)[19]. It effectively suppresses both bulk and surface diffusion of metallic impurities, thereby reducing contamination risks and providing a stable interfacial environment for superconducting quantum chips. Metals with strong diffusion resistance-such as Ta, Nb, TiN, and Ti-exhibit extremely low bulk diffusion coefficients in silicon-based dielectrics and high surface diffusion energy barriers, rendering their diffusion negligible at room temperature. In contrast, fast-diffusing elements like Au readily penetrate silicon through grain boundaries or defects, necessitating stringent contamination control. Aluminum (Al) may diffuse at elevated temperatures; however, quantum chip fabrication typically employs in-situ oxidation to form a dense 2-5 nm $Al_2O_3$ layer on metal lines, effectively inhibiting diffusion. Similarly, aluminum interconnects in conventional semiconductor back-end-of-line (BEOL) processes rely on a native oxide layer rather than additional diffusion barriers (e.g., TiN, TaN) to prevent leakage. For low-melting-point metals such as In/Sn, indium (In) exhibits rapid surface diffusion on Si (energy barrier ~0.31-0.66 eV) and tends to form a liquid-like film near its melting point[20]. Experimental observations have confirmed step-flow migration of In even at low temperatures (<100 ℃), requiring careful process control.

### 2.5.2 Suppression of Metal Diffusion by Process Environment

The low-temperature fabrication and operational environment of quantum chips substantially mitigates metal diffusion risks. Process temperatures are strictly limited (typically <250 ℃), effectively suppressing thermally activated diffusion. The operational environment operates at millikelvin (mK) temperatures, where thermodynamic driving forces are extremely low. Additionally, the driving current is only on the order of microamperes (μA)-three to five orders of magnitude lower than in conventional semiconductors-minimizing the risk of electric-field-induced diffusion.

### 2.5.3 Influence of Quantum Chip Structural Features

Compared with conventional semiconductors, quantum chips feature relatively simple

structures without complex three-dimensional architectures. The substrate primarily serves a mechanical support function and does not participate in device operation. However, air-gap isolation structures expose metal interconnects directly, introducing unique surface effects. During chip fabrication, surface states-including roughness and native oxide layers-significantly influence migration energy barriers. Consequently, surface treatments during processing (e.g., cleaning and passivation) directly impact long-term device stability. Although the operational vacuum environment maintains surface stability, initial contamination may still compromise device performance.

### 2.5.4 Experimental Study on Diffusion Characteristics of UBM Structures on Silicon Substrates

With advances in quantum computing technology, quantum chips with tens of qubits now commonly employ advanced three-dimensional packaging techniques such as flip-chip bonding. In such packaging configurations, the under bump metallization (UBM) layer serves as the critical interfacial layer connecting solder bumps to chip pads, and its reliability directly determines long-term device stability[21,22]. This study systematically investigates the mechanism by which metal diffusion from a Ti/Au-based UBM layer-overlapping with exposed regions of the silicon substrate-affects the substrate's insulating properties.

The experimental design employs a comb-type test structure (Figure 3) with the following dimensions: line spacing of 2 μm and line length of 200 × 200 μm. During sample preparation, the native oxide layer on the silicon surface was first removed via ion beam sputtering, followed by sequential electron-beam evaporation of 10 nm Ti and 200 nm Au. To simulate actual process conditions, the samples underwent a post-deposition thermal treatment at 245 ℃ for 5 min.

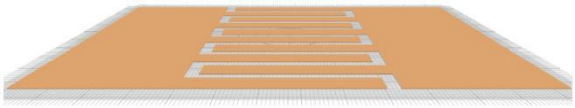

**Fig. 3 Schematic of interline resistance test structure for comb-shaped UBM electrodes.**

Figure 4 shows that the resistance measurements indicate an order-of-magnitude decrease in inter-wire resistance of the UBM after high-temperature treatment. This phenomenon confirms the physical process of Au atoms diffusing through the Ti barrier layer into the silicon substrate. To further investigate the diffusion mechanism, we conducted the following control experiments: First, increasing the Ti layer thickness to 20 nm yielded no significant improvement in barrier performance, indicating that merely thickening the Ti layer cannot effectively suppress Au diffusion.

Second, we introduced a 200 nm Ta barrier layer beneath the UBM and separately examined diffusion characteristics in the central and edge regions. Experimental data reveal that the surface diffusion of Au along the Ti layer exhibits diffusion intensity comparable to that of bulk diffusion through the Ti layer, with no significant surface-enhanced diffusion observed.

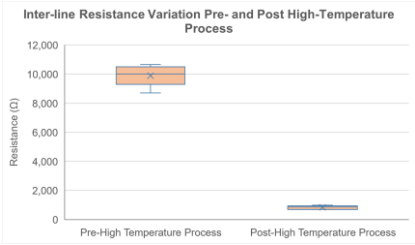


**Fig. 4 Comparison of UBM interline resistance before and after thermal treatment (245 °C/5 min).**

Initial experimental results suggest that non-primary materials (e.g., non-superconducting metals) should be included in the scope of investigation. Gold diffusion into the substrate may induce signal crosstalk or anomalous heating in quantum chips. However, an alternative possibility exists: when the quantum chip operates in its superconducting state, the change in silicon substrate resistivity caused by gold diffusion-being a non-superconducting metal-may be entirely negligible in comparison. Definitive conclusions require further systematic and in-depth research.

### 2.5.5 Unique Challenges in Metal Contamination Control for Quantum Chips

Compared with conventional semiconductor chips, contamination control for superconducting quantum chips presents several distinctive challenges. The fabrication process employs diverse materials, including multiple superconducting metals (e.g., Ta, Nb, Al, TiN), each exhibiting distinct diffusion characteristics. Moreover, the continuous introduction of novel superconducting materials necessitates ongoing assessment of contamination risks. Additionally, dielectric isolation schemes commonly used in semiconductor manufacturing cannot be directly adopted due to process constraints. Traditional purification techniques such as high-temperature annealing are also restricted by the stringent frequency stability requirements of qubits. Owing to the surface sensitivity of these materials, the diffusion behavior of exposed metal surfaces is closely tied to their surface chemical states. Process-induced surface modifications-such as oxidation or adsorption-can significantly impact long-term reliability.

## 2.6 Conclusions

Currently, sapphire substrates demonstrate the best resistance to diffusion among

available options for controlling metal contamination in quantum chips. For silicon substrates, particular attention must be paid to preventing diffusion of metals such as Au, In, and Sn. Furthermore, the low-temperature fabrication processes (<250 ℃) and ultra-cryogenic operating environments (millikelvin scale) employed in quantum chip manufacturing significantly suppress metal diffusion. The primary challenges today stem from exposed metal surfaces and material diversity, necessitating the development of a dedicated contamination control framework specifically tailored for quantum chips.

# 3 Research Status and Outlook

Current studies indicate that, under existing fabrication conditions, metal contamination has not yet become a primary bottleneck limiting quantum chip performance. The intrinsic properties of materials combined with the cryogenic operating environment jointly mitigate diffusion issues, while surface diffusion risks can be managed through optimized process parameters and surface treatments. Future research should prioritize evaluating the contamination characteristics of emerging superconducting materials, elucidating the mechanisms by which surface state engineering modulates migration behavior, and understanding surface evolution under long-term operational conditions. Concurrently, contamination control methodologies compatible with qubit performance must be developed. As quantum chips advance toward higher integration densities, establishing a standardized metal contamination assessment and control framework specifically for superconducting quantum devices will become increasingly critical.

Through sustained, multi-stakeholder collaborative efforts over many years, China's semiconductor industry achieved a major breakthrough in 2024 despite a deteriorating global trade environment and escalating international technology sanctions. Annual chip exports surpassed the RMB 1 trillion mark for the first time, and domestic supply capacity rose significantly to 30%. This milestone provides strong evidence of progress toward self-reliance and controllability in China's domestic semiconductor supply chain.

At present, China's quantum computing research stands at a pivotal stage of catching up with international frontiers. In response to technological blockades in chips, quantum technologies, and artificial intelligence, we must strengthen fundamental research, cultivate specialized talent, overcome critical fabrication challenges, and drive independent innovation in quantum computing. With continued national policy support and concerted efforts by researchers, the realization of a universal quantum computer is no longer a distant prospect.

## References


[1] Acharya R, Abanin D A, Aghababaie-Beni L, Aleiner I, Andersen T I, Ansmann M, Arute F, Arya K, Asfaw A, Astrakhantsev N, et al. 2025 *Nature* **638** 920

[2] Gao D X, Fan D J, Zha C, Bei J H, Cai G Q, Cai J B, Cao S R, Chen F S, Chen J, Chen K, et al. 2025 *Phys. Rev. Lett.* **134** 090601

[3] Van Damme J, Massar S, Acharya R, Ivanov T, Perez Lozano D, Canvel Y, Demarets M, Vangoidsenhoven D, Hermans Y, Lai J G, Vadiraj A M, Mongillo M, Wan D, De Boeck J, Potočnik A, De Greve K 2024 *Nature* **634** 74

[4] Dieter K S 2005 *Semiconductor Material and Device Characterization* （Hoboken: Wiley IEEE Press） p127

[5] Weber E R 1983 *Appl. Phys. A* **30** 1

[6] Quirk M, Serda J （translated by Han Z S） 2015 *Semiconductor Manufacturing Technology* （Beijing: Publishing House of Electronics Industry

[7] Xiao H 2012 *Introduction to Semiconductor Manufacturing Technology* （Bellingham: SPIE Press

[8] Mehrer H 2007 *Diffusion in Solids: Fundamentals, Methods, Materials, Diffusion-Controlled Processes* （Heidelberg: Springer Verlag

[9] Seshan K 2012 *Handbook of Thin Film Deposition: Techniques, Processes, and Technologies* （Amsterdam: Elsevier

[10] Gas P, d'Heurle F M 1993 *Appl. Surf. Sci.* **73** 153

[11] Nicolet M A 1978 *Thin Solid Films* **52** 415

[12] Gösele U, Frank W, Seeger A 1980 *Appl. Phys.* **23** 361

[13] Nakashima K, Iwami M, Hiraki A 1975 *Thin Solid Films* **25** 423

[14] Murarka S P 2005 *Diffusion Processes in Advanced Technological Materials* （Amsterdam: Elsevier） pp239–281

[15] Saiz E, Cannon R M, Tomsia A P 1999 *Acta Mater.* **47** 4209

[16] Matthews T S, Sawyer C, Ogletree D F, Liliental-Weber Z, Chrzan D C, Wu J 2012 *Phys. Rev. Lett.* **108** 096102

[17] Prabriputaloong K, Piggott M R 1973 *J. Am. Ceram. Soc.* **56** 177

[18] Seebauer E G, Allen C E 1995 *Prog. Surf. Sci.* **49** 265

[19] Kirby K W 2008 *M. S. Thesis* （State College: The Pennsylvania State University

[20] Wu N J, Yasunaga H, Natori A 1992 *Appl. Surf. Sci.* **260** 75

[21] Li Z R 2012 *M. S. Thesis* （Beijing: Beijing University of Chemical Technology

[22] Lu Y D, He X Q, En Y F, Wang X, Zhuang Z Q 2010 *Acta Phys. Sin.* **59** 3438