Electro-thermal modeling of self-heating effects in multi-channel GaN HEMTs and optimization of field plate structures*

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Abstract Multi-channel GaN HEMTs enhance the overall device performance by vertically stacking multiple AlGaN/GaN heterojunctions. This structure increases the total two-dimensional electron gas (2DEG) concentration while maintaining high mobility in each channel. However, it also introduces complex self-heating challenges. Although current sharing among multiple channels reduces the average heat flux per channel, the dense vertical stacking leads to significant inter-channel thermal coupling. This coupling particularly impairs heat dissipation in the middle channels, resulting in severe non-uniform temperature distribution. The gate-drain region sustains both high current density and high electric field, causing a concentrated heat flux distribution, thereby further exacerbating self-heating effects. To address these issues, this work proposes a bidirectional electro-thermal coupling model for multi-channel GaN HEMTs. The model self-consistently solves the drift-diffusion equations and the Fourier heat conduction equation. Bidirectional coupling is achieved by incorporating the temperature dependence of carrier mobility. This approach accurately characterizes the electro-thermal distribution of the device. Simulation results reveal significant vertical thermal coupling between adjacent channels. The middle channel exhibits the most severe temperature rise, with its temperature approximately 15 – 20 K higher than that of edge channels under typical operating conditions. Moreover, the current density degradation due to self-heating in the hottest channel reaches a significant level, demonstrating the necessity of coupled simulation. Based on the advantages of field plates in optimizing electric field distribution and improving breakdown voltage, this study further explores their feasibility in suppressing self-heating by modulating the channel electric field. The effects of four different

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gate-drain field plate structures on electric field and heat flux distribution are systematically evaluated. Results show that the slanted field plate is the most effective configuration. Its underlying mechanism lies in transforming the single large potential drop concentrated at the gate edge into multiple gradual steps along the channel. This smoothes the electric field distribution and significantly reduces the peak heat flux density. Through parametric optimization, an optimal configuration with a 6° slant angle and a 1.2 μm length is identified. Compared to the structure without a field plate, this design reduces the peak electric field and peak heat flux density by approximately 75%. The maximum channel temperature decreases from 472.8 K to 461.9 K, a reduction of about 6%, while the device's electrical performance remains largely unaffected. This study provides critical insights into the unique electro-thermal coupling mechanisms in multi-channel GaN HEMTs. It also demonstrates that optimally designed slanted field plates offer an effective approach for enhancing the thermal reliability of high-performance GaN power devices.

Keywords electro-thermal coupling; GaN high electron mobility transistor; multi-channel; field plate structure
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1 Introduction

Gallium nitride high-electron-mobility transistors (GaN HEMTs) are widely used in communication, radar, and space systems due to their high operating frequency, high breakdown voltage, high electron saturation velocity, low on-resistance, and excellent thermal properties[1-4]. The superior performance of these devices stems from the two-dimensional electron gas (2DEG) induced by polarization effects at the AlGaN/GaN interface. This 2DEG achieves a carrier concentration exceeding 1×10^{13} cm^{-2} at room temperature[5] and a carrier mobility greater than 2000 $cm^2/(V\ s)$[6]. However, in traditional single-channel structures, carrier scattering mechanisms cause the mobility to decrease as the 2DEG concentration increases, thereby restricting further improvement in device performance.

To overcome the inherent trade-off between carrier concentration and mobility, multi-channel GaN HEMT devices vertically stack multiple AlGaN/GaN heterojunction structures. This approach increases the total 2DEG concentration while maintaining the carrier mobility in each channel, effectively enhancing overall device performance[7,8]. However, the multi-channel structure introduces significant thermal reliability challenges alongside improved electrical performance[9]. The heterojunctions beneath the channels in multi-channel GaN HEMTs deplete the 2DEG

within the channels, reducing the 2DEG concentration. According to Joule's law ($Q = \boldsymbol{J} \cdot \boldsymbol{E}$)[10], the heat flux density in a single channel of a multi-channel GaN HEMT is lower than that in a single-channel GaN HEMT under the same bias voltage. Nevertheless, the region beneath the intermediate channels in multi-channel devices consists of adjacent channels rather than conventional buffer layers. As the channels are the primary heat sources, their dense stacking hinders effective heat dissipation from the intermediate channels. This results in thermal coupling, rendering the heat dissipation conditions in this region significantly worse than those at the edge channels. Such thermal non-uniformity exacerbates local temperature rise, thereby affecting the electrical characteristics and thermal reliability of the device[11]. Therefore, precise control of heat flux density distribution in multi-channel GaN HEMTs is crucial for suppressing self-heating effects and ensuring stable device operation. In the gate-drain region of multi-channel GaN HEMTs, the coexistence of high current density and high electric field strength leads to a significant increase in local heat flux density, causing severe self-heating effects. Since high current is an inherent characteristic of multi-channel structures for achieving high performance and is difficult to regulate further, the key to suppressing self-heating lies in optimizing the electric field distribution in this region to reduce local heat flux density. As a critical component between the gate and drain, the field plate structure can effectively optimize the electric field distribution at the gate edge[12-16], providing a viable path for suppressing self-heating effects.

Based on this, this study focuses on the gate-drain field plate structure to effectively suppress self-heating effects in multi-channel devices. Although existing studies have explored the impact of field plates on the temperature distribution of single-channel GaN HEMTs[17-20], thermal coupling effects in multi-channel GaN HEMTs are more complex, and local overheating issues are more prominent compared to single-channel devices. Currently, systematic electro-thermal coupling research specifically for multi-channel devices remains scarce. To address this, we constructed an electro-thermal coupling model suitable for multi-channel GaN HEMTs. By coupling the drift-diffusion equations with the Fourier heat conduction equation and incorporating the temperature dependence of mobility, we accurately characterized the electro-thermal distribution of the device under steady-state operating conditions and revealed the vertical thermal coupling effects between channels. Based on this work, we systematically evaluated the impact of four gate-drain field plate structures on the electric field and heat flux density distribution within the channels. We investigated the mechanism by which slanted field plates optimize electric field distribution and suppress self-heating by decomposing concentrated potential jumps into multiple gradual steps. This provides technical support for the structural design of multi-channel GaN HEMTs. The remainder of this paper is organized as follows: Section 2 details the

device structure and the establishment and verification methods of the electro-thermal coupling model. Section 3 first analyzes the impact of channel number on the electro-thermal characteristics of the device, then studies the suppression effect of gate-drain field plates on self-heating effects, with a focus on the optimization role of the tilt angle and length of slanted field plates in improving device thermal behavior. Section 4 summarizes the research findings and discusses prospects for further investigating thermal coupling effects in multi-channel structures using non-Fourier heat conduction models.

2 Research Methods and Device Configuration

2.1 Device Geometric Model

The device structure involved in this study is shown in Fig. 1(a). From bottom to top, the layers are: a 400-μm-thick sapphire substrate, a 100-nm-thick aluminum nitride (AlN) nucleation layer, a 1.5-μm-thick gallium nitride (GaN) buffer layer, a 5 nm thick GaN channel layer, a 20 nm thick aluminum gallium nitride ($Al_{0.25}Ga_{0.75}N$) barrier layer, and a 148 nm thick silicon nitride (SiN) passivation layer. The background doping concentration for both the barrier and channel layers is 1×10^{15} cm^{-3}. Multi-channel devices are formed by repeatedly stacking barrier and channel layers. For example, a three-channel device contains three barrier layers and three channel layers (repeated three times), while a five-channel device contains five barrier layers and five channel layers (repeated five times). The gate length of the metal gate is 1 μm, the gate-source spacing (L_{GS}) is 1 μm, and the gate-drain spacing (L_{GD}) is 3 μm. An ideal lattice is assumed, and the influence of trap effects is neglected. Fig. 1(b) shows the schematic of the thermal boundary conditions for the model. Figs. 1(c)-(f) display the schematic diagrams of the four gate-drain field plate structures used in this study: conventional field plate, slanted field plate, stepped field plate, and discrete field plate. Each field plate structure was designed according to previous studies[21-24]. To maintain comparability, the length of all gate-drain field plates was fixed at 1.2 μm.

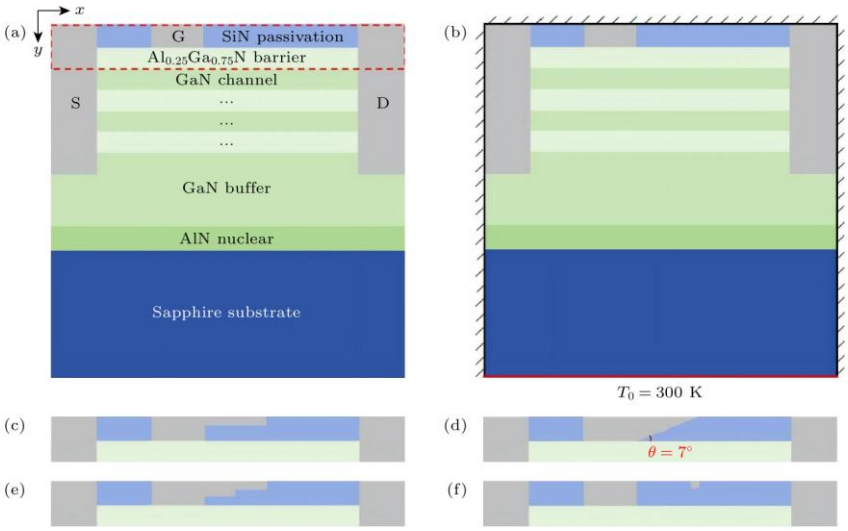


Fig. 1 Schematic diagrams of the simulation model: (a) Multi-channel GaN HEMT device; (b) thermal boundary conditions; (c) conventional field plate; (d) slanted field plate; (e) stepped field plate; (f) discrete field plate.

2.2 Electro-thermal Coupling Model

This study establishes a two-dimensional electro-thermal coupling model for multi-channel GaN HEMT devices based on the TCAD platform. The model neglects thickness along the gate width direction. In practice, the device exhibits an aspect ratio of 1:100. This large aspect ratio renders the central region approximately symmetric in electro-thermal behavior. Consequently, a two-dimensional cross-section effectively characterizes the primary physical processes in this region. In the actual three-dimensional structure, the device periphery is subject to air natural convection boundaries, while the substrate bottom connects to a constant-temperature heat sink. As the device is planar, its vertical dimensions are significantly smaller than its horizontal dimensions. Heat primarily conducts downward through the substrate. Estimates indicate that the thermal resistance along the gate width direction (approximately 10^5 K/W) far exceeds the vertical thermal resistance (approximately 10^2 K/W). Under steady-state operating conditions, the horizontal temperature gradient is smaller than the vertical gradient. Analysis based on one-dimensional steady-state heat transfer and structural symmetry suggests that heat diffusion along the gate width has a negligible impact on self-heating effects in the central device region. Since this study focuses on vertical thermal coupling between channels and the influence of field plate structures on electro-thermal characteristics in the gate-drain region, this simplification does not substantially affect the relevant conclusions. The platform solves the coupled partial differential equations in the electro-thermal model, including drift-diffusion and heat conduction equations, using the finite volume method. The electric potential and field distributions within the device are described by the Poisson equation, electron transport

equation, and hole transport equation[25]:

$$\nabla^2\phi = -\frac{q}{\varepsilon}(p - n + N_{\mathrm{D}} - N_{\mathrm{A}}), \tag{1}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \boldsymbol{J}_n - (R - G), \tag{2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \cdot \boldsymbol{J}_p - (R - G), \tag{3}$$

Here, $\boldsymbol{J}_n$ and $\boldsymbol{J}_p$ denote the electron and hole current densities, respectively; $(R - G)$ represents the net generation or recombination rate of electrons and holes; q is the elementary charge; ε is the dielectric constant; ϕ is the electric potential; n and p are the electron and hole concentrations, respectively; and N_{D} and N_{A} are the concentrations of ionized donor and acceptor impurities, respectively. The simulation also accounts for the polarization charge σ arising from polarization effects in AlGaN/GaN, which is expressed as[26]

$$|\sigma(x)| = \left|2\frac{a(x)-a(0)}{a(0)}\left\{e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)}\right\} + P_{\mathrm{SP}}(x) - P_{\mathrm{SP}}(0)\right|, \tag{4}$$

Here, x denotes the Al mole fraction in $Al_xGa_{1-x}N$, with $x = 0.25$. In this case, a represents the lattice constant; e_{31} and e_{33} are the piezoelectric coefficients; C_{13} and C_{33} are the elastic coefficients; and P_{SP} is the spontaneous polarization intensity.

By employing the classical drift-diffusion equations, the electron and hole current densities within the device can be expressed as[10]

$$\boldsymbol{J}_n = -q\mu_n n\boldsymbol{E} + qD_n\nabla n, \tag{5}$$

$$\boldsymbol{J}_p = -q\mu_p p\boldsymbol{E} - qD_p\nabla p, \tag{6}$$

Here, μ_n and μ_p denote the electron and hole mobilities, respectively; $\boldsymbol{E}$ represents the electric field intensity; and D_n and D_p are the electron and hole diffusion coefficients, respectively, which can be expressed as[27]

$$D_n = \frac{k_{\mathrm{B}}T}{q}\mu_n, \tag{7}$$

$$D_p = \frac{k_{\mathrm{B}}T}{q}\mu_p, \tag{8}$$

Here, T denotes the internal device temperature, and k_{B} represents the Boltzmann

constant. To better analyze the electrical performance of the device under actual operating conditions, it is necessary to consider the internal temperature distribution. Therefore, we introduce the energy equation based on Fourier heat conduction[28]:

$$C\frac{\partial T}{\partial t} = \nabla(\kappa\nabla \cdot T) + Q, \tag{9}$$

Here, κ denotes the thermal conductivity of the material; C represents the heat capacity; and Q indicates the internal heat source within the device, expressed as[29]

$$\begin{aligned} Q = \ & \frac{|J_n|^2}{q\mu_n n} + \frac{|J_p|^2}{q\mu_p p} + q(R-G)[\phi_p - \phi_n + T_{\mathrm{L}}(P_n - P_p)] \\ & -T_{\mathrm{L}}(J_n \cdot \nabla P_n + J_p \cdot \nabla P_p), \end{aligned} \tag{10}$$

Here, P_n and P_p denote the absolute thermoelectric power of electrons and holes, respectively.

In addition to the drift-diffusion and heat conduction equations, the simulation incorporates the Shockley-Read-Hall (SRH) recombination model[30] to describe carrier generation and recombination processes:

$$R^{\mathrm{SRH}} = \frac{n\cdot p - n_{\mathrm{i}}^2}{\tau_p\cdot(n+n_{\mathrm{i}}) + \tau_n\cdot(p+p_{\mathrm{i}})}, \tag{11}$$

Here, τ_n and τ_p denote the carrier lifetimes for electrons and holes, respectively; n_{i} and p_{i} represent the intrinsic carrier concentrations for electrons and holes. To accurately describe carrier transport behavior, the model accounts for the effects of temperature and inter-carrier scattering on mobility. It employs a field-dependent mobility model and a velocity saturation model to characterize carrier transport in the device active region under high electric fields[31]. The carrier mobilities follow Mathiessen's rule[32]:

$$\frac{1}{\mu_{\mathrm{low}}} = \frac{1}{\mu_{\mathrm{L}}} + \frac{1}{\mu_{\mathrm{I}}}, \tag{12}$$

$$\mu_{\mathrm{L}} = \mu_{300}(300/T)^{\varsigma}, \tag{13}$$

$$\mu_{\mathrm{I}} = \mu_{min1}\exp\left(-\frac{P_{\mathrm{c}}}{N}\right) + \frac{\mu_{\mathrm{L}} - \mu_{min2}}{1+(N/C_{\mathrm{r}})^{\varepsilon_1}} - \frac{\mu_1}{1+(C_{\mathrm{s}}/N)^{\varepsilon_2}}, \tag{14}$$

$$\mu(F) = \frac{\mu_{\mathrm{low}}}{[1+(\mu_{\mathrm{low}}\cdot F/v_{\mathrm{sat}})^{\beta}]^{1/\beta}}, \tag{15}$$

Here, μ_{low} denotes the low-field carrier mobility; μ_{L} represents the carrier mobility under temperature influence; μ_{I} indicates the carrier mobility caused by carrier scattering; μ_{300} is the carrier mobility of the material at the reference temperature of 300 K; ς is the coefficient for the temperature dependence of carrier mobility, with $\varsigma = 2.5$; μ_{min1}, μ_{min2}, and μ_1 are reference mobilities; P_{c}, C_{r}, and C_{s} represent standard doping concentrations; N is the net doping concentration; the power exponents are $\varepsilon_1 = 0.55$ and $\varepsilon_2 = 0.75$; v_{sat} denotes the carrier saturation velocity; β is a temperature-dependent coefficient, with $\beta = 1.7$; and F represents the carrier driving force in the device, namely the quasi-Fermi level gradient, which can be expressed as[33]

$$F = |\nabla \phi_{n(p)}|, \tag{16}$$

Here, ϕ_n and ϕ_p denote the quasi-Fermi potentials for electrons and holes, respectively.

Furthermore, the temperature dependence of the thermal conductivity of GaN is considered, as expressed below:

$$\kappa = \kappa_{300}(300/T)^{\alpha}, \tag{17}$$

Here, κ_{300} denotes the reference thermal conductivity of GaN at $T = 300\mathrm{K}$; α represents the coefficient governing the temperature dependence of thermal conductivity, with $\alpha = 1.4$. Table 1 lists the other model parameters used in the simulation.

Table 1 Key parameters used in the simulations.

Parameter	GaN	AlN	Sapphire
Band gap/eV	3.4	6.2	8.8
Relative dielectric constant	8.9	8.5	9.3
Electron mobility/(cm2·V-1·s-1)	1840	300	-
Electron saturation velocity/(cm·s-1)	2×107	7.7×106	-
Thermal conductivity/(W·cm-1·K-1)	2.1	0.1	5.5

The thermal boundary conditions employed in the simulation are illustrated in Fig. 1(b). Given the excellent thermal insulation of the top passivation layer, the upper surface is defined as an adiabatic boundary. Since heat generated by the device primarily dissipates downward through the substrate, the bottom surface of the substrate is set as a constant temperature boundary at $T_0 = 300\mathrm{K}$. Additionally, the lateral sides of the device are assigned adiabatic boundaries as lateral heat diffusion is negligible compared to vertical heat dissipation[34]. Regarding electrical boundary conditions, the

source and drain electrodes are configured as Ohmic contacts to simulate efficient carrier injection at the metal-semiconductor interfaces. The gate electrode is modeled as a Schottky contact to capture its rectifying and modulating effects on the channel. The electric potential at these electrode interfaces is maintained at constant values. All remaining surfaces are defined as electrically insulated boundaries to simulate the physical environment where the device is surrounded by passivation layers or air[32].

2.3 Model Validation

A graded meshing strategy was employed when constructing the simulation model for the GaN HEMT device. The finest mesh elements were applied to the region near the drain-side edge of the gate, where the electric field intensity is highest. To accurately characterize the polarization effects at the AlGaN/GaN heterojunction interface, a dense parallel mesh was adopted at the interface. The channel region also underwent mesh refinement to precisely describe current and temperature distributions. To enhance computational efficiency, coarser meshes were applied to non-critical areas such as the substrate. A mesh independence study was conducted to balance computational accuracy and efficiency. Simulations were performed using six different mesh densities: 2.6×10^4, 4.3×10^4, 5.0×10^4, 7.2×10^4, 10.1×10^4, and 12.0×10^4 elements. The maximum device temperature and output current were extracted for analysis. As shown in Fig. 2, when the mesh count increased from 7.2×10^4 to 10.1×10^4, the relative variations in both parameters remained below 0.01%, indicating convergence. Consequently, the mesh scheme with 7.2×10^4 elements was selected for the final simulations, effectively conserving computational resources while ensuring accuracy.

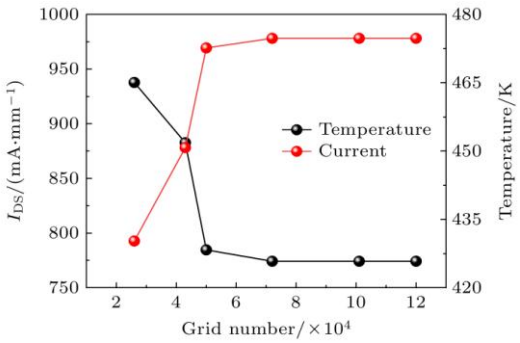


Fig. 2 Mesh independence study.

To rigorously assess the reliability of the numerical model, we calibrated the electro-thermal bidirectional coupling model using experimental data[34,35]. We employed a Keysight 4200 semiconductor parameter analyzer to test the basic electrical characteristics of the device at room temperature, including output and transfer characteristic curves. For the output characteristic tests, we fixed the gate voltages at 0.0, -2.0, and -4.0 V while sweeping the drain voltage from 0.0 V to 10.0 V. In the

transfer characteristic tests, we maintained the drain voltage at 10.0 V and swept the gate voltage from 0.0 V to -12.0 V. Figure 3(a) compares the simulated and measured results for the device output characteristics. The simulation curves align well with the experimental data under various gate voltages, thereby validating the accuracy of the established electro-thermal coupling model. Furthermore, to investigate the electrical properties of multi-channel GaN HEMT devices, Figure 3(b) presents the transfer characteristic curves and transconductance of a dual-channel device. The transconductance curves exhibit multiple peaks, which correspond to the threshold voltages for channel activation. This multi-peak distribution aligns with the transport behavior of multi-channel devices reported in previous studies, indicating that the simulated device possesses the typical characteristics of a multi-channel structure.

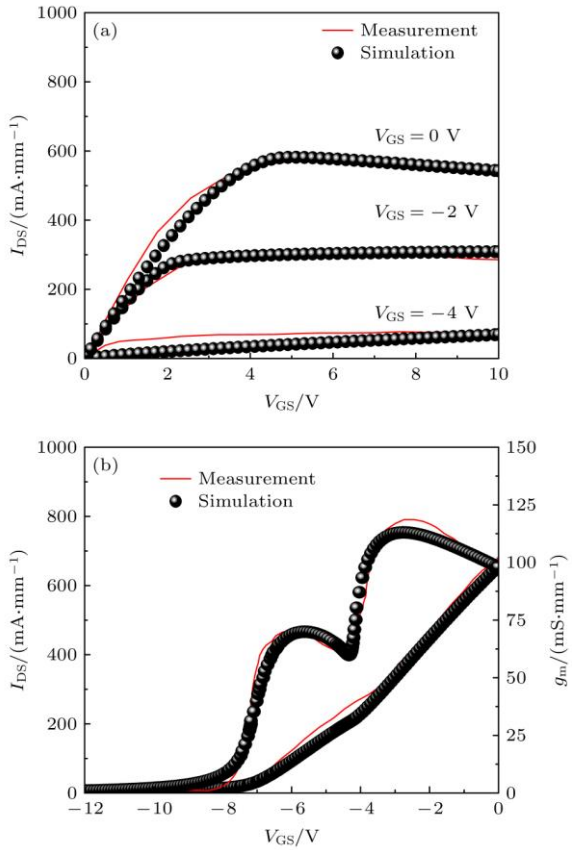


Fig. 3 (a) Comparison of output characteristic curves; (b) comparison of transconductance characteristics. The symbols represent the simulation results, and the solid lines denote the results obtained from the electro-thermal coupling model developed in this study.

3 Results and Analysis

3.1 Impact of Channel Count on Device Performance

This section analyzes the impact of channel count on the performance of GaN HEMT devices. Unlike traditional single-channel devices, multi-channel GaN HEMTs

integrate additional AlGaN/GaN heterojunctions beyond the single heterojunction structure. As shown in Fig. 4, the built-in electric fields generated by polarization effects between these heterojunctions cause the conduction band edge at the interface near the GaN channel layer to bend below the Fermi level, thereby forming multiple quantum wells. Free electrons induced by positive polarization charges are confined within these quantum wells, creating a high-concentration two-dimensional electron gas (2DEG) in the GaN channel layer. Notably, the introduction of multiple heterojunctions is equivalent to adding a back-barrier layer to the original channel. This exerts a depletion effect on the 2DEG in the channel layer, leading to a reduction in the 2DEG concentration within each individual channel. Figure 5 illustrates the impact of channel count on carrier mobility within a single channel and the total 2DEG concentration of the device. The results indicate that although the 2DEG concentration in a single channel decreases, the total 2DEG concentration in the device increases due to the higher number of channels. Carrier mobility within each single channel shows no significant change compared to single-channel devices. This finding suggests that the multi-channel structure overcomes the inherent trade-off between carrier concentration and mobility, maintaining favorable transport properties while enhancing carrier concentration.

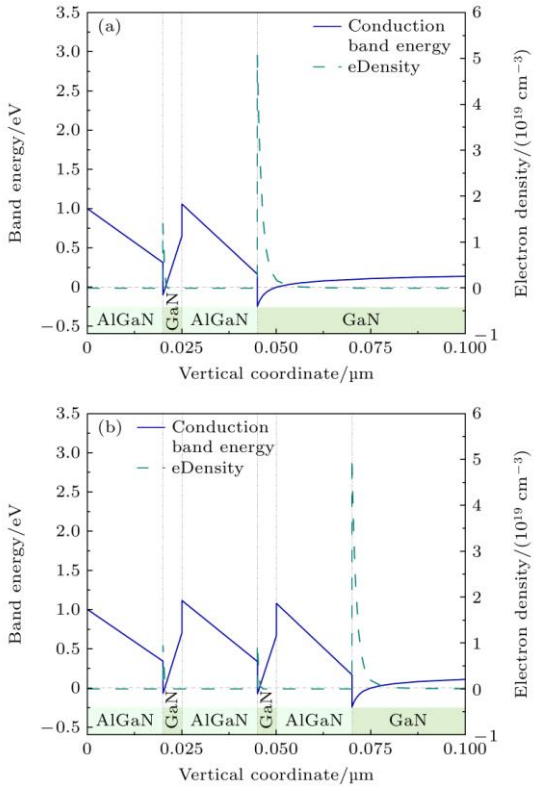


Fig. 4 Band structure and electron concentration distribution of the devices: (a) Dual-channel device; (b) triple-channel device.

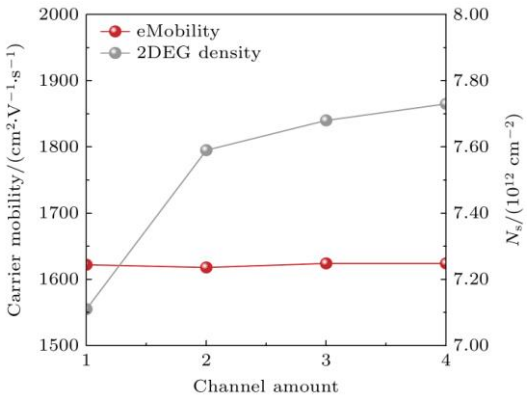


Fig. 5 Effect of the number of channels on carrier mobility in individual channels and total 2DEG density.

Following the above analysis, Figure 6 illustrates the variation of device saturation current with the number of channels. The device saturation current increases significantly with the number of channels and gradually approaches saturation. This phenomenon primarily stems from two factors. First, the continuous increase in channel count weakens the gate control over channel switching, thereby limiting further growth in saturation current[36]. However, this limitation can be mitigated by introducing an appropriate back-barrier structure in the bottom channel. Second, high saturation current is accompanied by a significantly enhanced self-heating effect. Simulation results indicate that the maximum internal channel temperature rises markedly from 433.7 K to 488.4 K as the number of channels increases. This occurs because, at the same source-drain bias, the increased number of channels raises the total current, causing electric field concentration between the gate and drain electrodes, leading to a sharp rise in power dissipation and substantial Joule heating. The resulting temperature rise within the channel intensifies electron scattering, which significantly reduces channel electron mobility and ultimately constrains the electrical performance of the device.

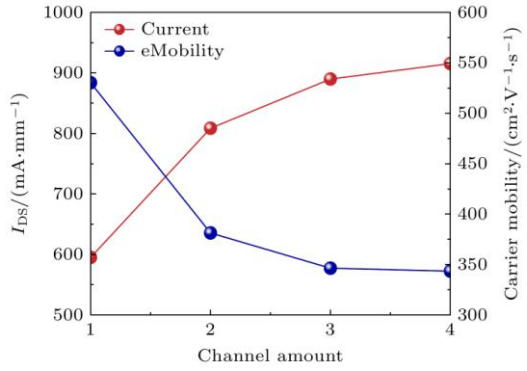


Fig. 6 Effect of the number of channels on saturation current and saturation region electron mobility.

To further analyze the internal temperature distribution profiles of the device, we performed a cross-sectional analysis along the vertical direction at the gate edge near the drain terminal of the GaN HEMT. Figure 7 illustrates the variation of the dimensionless temperature $T^* = (T - T_{min})/(T_{max} - T_{min})$ along the vertical axis of the device. Observations indicate that the temperature increases with depth in the barrier and channel layers but decreases upon entering the buffer layer. This temperature distribution profile primarily stems from the operating mechanism of the GaN HEMT. The voltage applied between the source and drain creates a lateral electric field at the AlGaN/GaN heterojunction interface, driving the transport of the two-dimensional electron gas (2DEG) to form a current path. The electric field intensity reaches its maximum at the heterojunction interface near the drain-side gate edge. This strong electric field accelerates electrons to velocity saturation or even velocity overshoot. As Joule heating constitutes the primary heat source in the device, the superposition of high electric field strength and high current density significantly increases the local thermal power density, thereby raising the temperature, as described by Joule's law $Q = \boldsymbol{J} \cdot \boldsymbol{E}$[10]. Meanwhile, owing to the high thermal conductivity of GaN, heat diffuses effectively toward the substrate, causing the temperature in the buffer layer region to decrease. The results demonstrate that the temperature field distribution patterns are fundamentally consistent across devices with different channel counts. The highest temperature consistently occurs in the conductive channel region at the AlGaN/GaN heterojunction interface. However, significant differences exist in the temperature distribution among the individual channels. As shown in Figure 7(a), the temperature of the lower channel in the dual-channel device is higher than that of the upper channel. This discrepancy arises because the lower channel has a higher 2DEG concentration. The high carrier concentration increases the local heat flux density, generating more Joule heat. In contrast, the three-channel structure shown in Figure 7(b) exhibits a different temperature distribution characteristic. The middle channel has the highest temperature, followed by the upper channel, while the lower channel has the lowest temperature. The primary cause of this difference is the impaired heat dissipation condition of the middle channel. Specifically, as the number of channels increases, the heat dissipation conditions for the middle channel change significantly. In single-channel devices, the channel is directly adjacent to the buffer layer, allowing effective vertical heat diffusion. In multi-channel devices, however, the middle channel is affected by thermal coupling from the adjacent upper and lower channels. This impaired heat dissipation hinders effective heat removal, resulting in a higher temperature in the middle channel compared to its neighbors. Notably, although Figure 4(b) shows that the 2DEG concentration in the third channel is higher than that in the middle channel, its temperature is lower. This indicates that in multi-channel structures, thermal coupling effects and differences in heat dissipation conditions, rather than

solely the 2DEG concentration, become the key factors governing the temperature distribution.

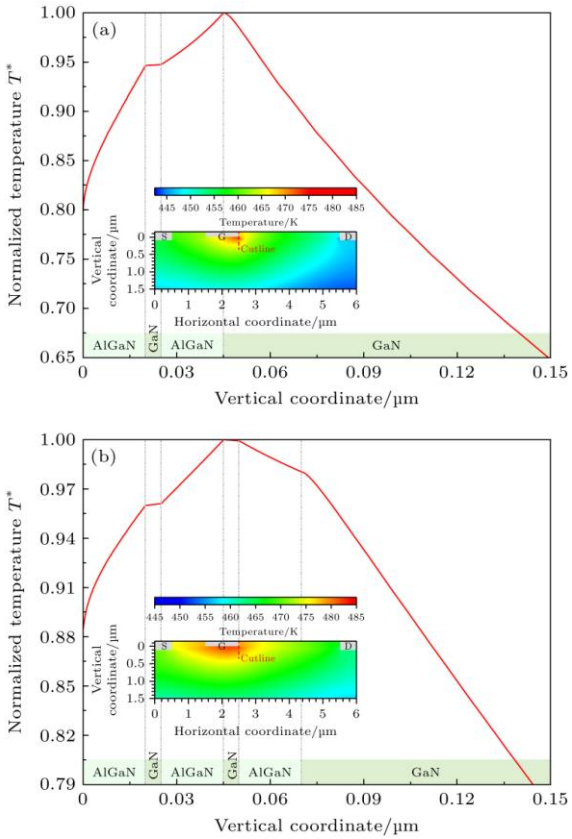


Fig. 7 V_{GS} = 0 V, V_{DS} = 10 V, internal temperature variation of the device: (a) Dual-channel device; (b) triple-channel device.

3.2 Impact of Field Plate Structures on Self-Heating Effects

To suppress self-heating effects, we investigated the influence of four different field plate structures in the gate-drain region. This region exhibits the highest electric field intensity and thus the maximum heat flux density. The study relied on the established electro-thermal coupling model. Using a dual-channel GaN HEMT as the device under study, we systematically compared the effects of conventional, slanted, stepped, and discrete field plate structures on device self-heating. Figure 8 illustrates the potential distribution beneath the field plates for devices with these four structures under identical bias conditions (V_{GS} = 0 V, V_{DS} = 10 V). The results indicate that devices with slanted field plates exhibit a smoother potential distribution across the entire field plate region, with potential changing uniformly along the slanted surface. In contrast, the other three field plate structures show abrupt potential changes near the drain-side edge of the gate. This phenomenon arises from the geometric structure at the connection between the field plate and the gate, which causes abrupt changes in the potential gradient. In conventional, stepped, and discrete field plate structures, the sidewalls of

the metal gate are vertical. To terminate electric field lines from the channel, a large amount of charge concentrates in the small area at the bottom of the vertical edge. This concentration leads to uneven local electric field distribution. Further analysis based on the parallel plate capacitor model reveals that the potential in this region must change abruptly over a very short distance. This requirement further exacerbates the non-uniformity of the electric field distribution. The combined action of these two mechanisms ultimately results in a significant potential gradient in the edge region of the gate near the drain. The slanted field plate structure converts the vertical edge into a slanted conductive surface. This design allows the originally concentrated charge to distribute uniformly over a longer path, thereby improving the electric field distribution. Furthermore, the slanted field plate can be viewed as a series of continuous micro-steps. This configuration decomposes one large potential jump into multiple small steps. Each micro-step accounts for only a small fraction of the total potential difference. Consequently, this configuration achieves a smoother local potential transition, effectively suppresses the peak local electric field intensity, and enhances the uniformity of the electric field distribution[37]. Figure 9 further presents the internal temperature distribution of the devices corresponding to the four field plate structures. Compared to the maximum temperature of the device without a field plate (472.8 K), all field plate structures effectively reduce the maximum device temperature. The recorded temperatures are 470.2 K (conventional field plate), 466.4 K (slanted field plate), 469.3 K (stepped field plate), and 470.5 K (discrete field plate). Among these, the slanted field plate demonstrates the most significant suppression of maximum temperature rise. This finding indicates that improving the electric field distribution effectively mitigates device self-heating effects. Although local hot spots in the device remain primarily concentrated in the region between the gate and drain electrodes, the slanted field plate structure exhibits significant thermal management advantages.

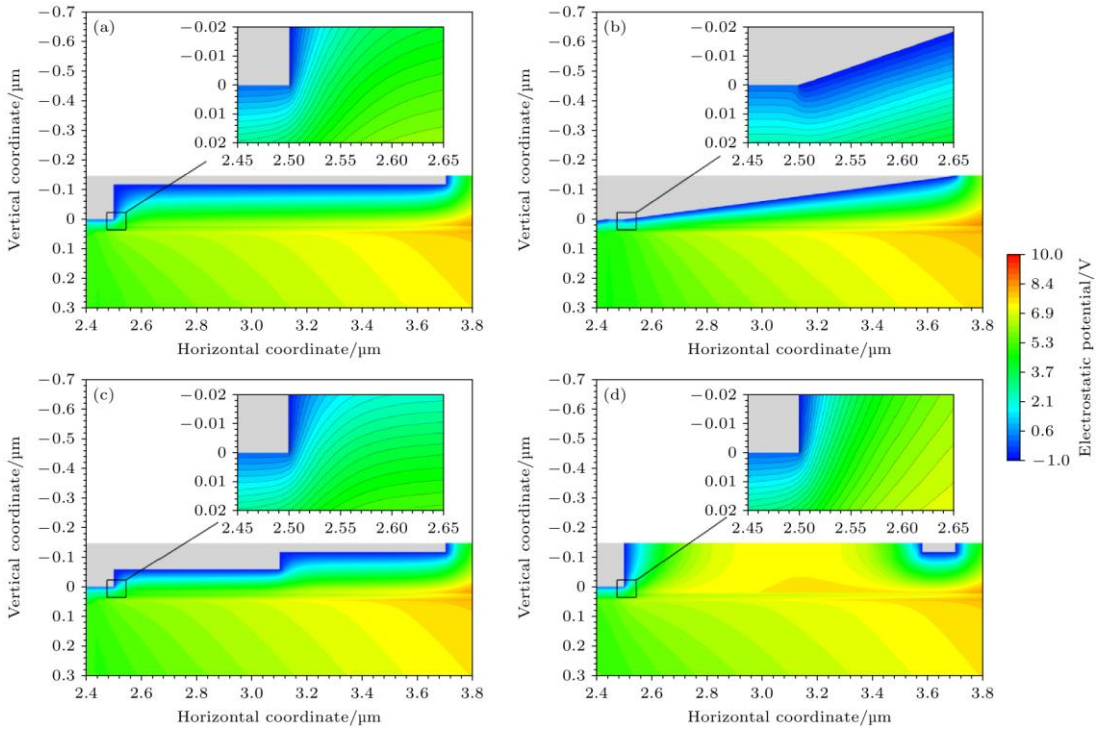


Fig. 8 V_{GS} = 0 V, V_{DS} = 10 V, potential distribution beneath the field plate: (a) Conventional field plate; (b) slanted field plate; (c) stepped field plate; (d) discrete field plate.

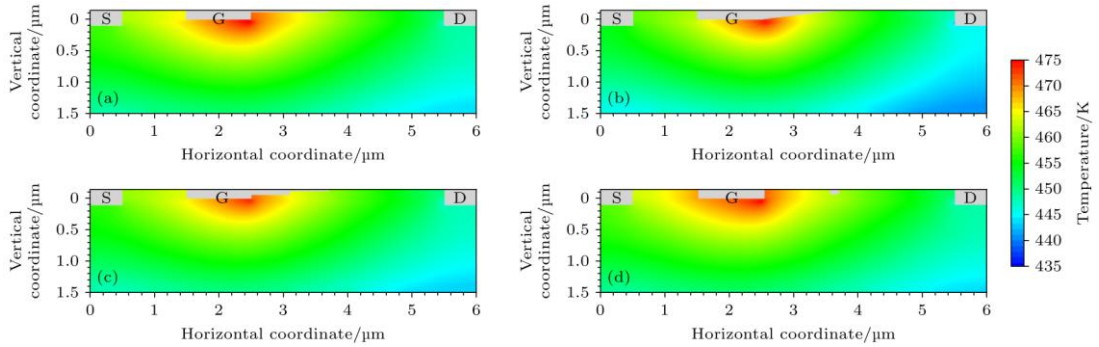


Fig. 9 V_{GS} = 0 V, V_{DS} = 10 V, device temperature distribution: (a) Conventional field plate; (b) slanted field plate; (c) stepped field plate; (d) discrete field plate.

To further investigate the mechanism by which the slanted field plate influences the thermal distribution of the device, Figure 10(a) compares the heat flux density in each channel of the dual-channel GaN HEMT under conventional and slanted field plate structures. The results indicate that the heat flux density in the lower channel is significantly higher than that in the upper channel under both field plate configurations. This difference is primarily attributed to the higher two-dimensional electron gas (2DEG) concentration in the lower channel. Furthermore, the slanted field plate structure effectively reduces the peak heat flux density. Specifically, the peak heat flux density decreases by 50% in the upper channel and by 30% in the lower channel. Integration along the channel direction reveals that the difference in total power

dissipation between the two field plate structures is only approximately 3%. This finding suggests that the reduction in peak temperature stems mainly from the optimization of heat source distribution rather than a significant change in total device power dissipation. A further analysis of the physical origin indicates that, given the approximately uniform lateral current density in the channel, variations in heat flux density are primarily associated with the lateral electric field distribution. As shown in Figure 10(b), compared with the structure without a field plate, the device with a slanted field plate exhibits a second, smaller peak in electric field strength at the edge of the field plate[38]. This phenomenon demonstrates that the slanted field plate can effectively homogenize the electric field distribution and suppress local electric field intensity by modulating the channel charge and potential distribution[37]. Simulation results show that under the influence of the slanted field plate, the peak lateral electric field strength at 1 nm below the channel decreases significantly from 0.47 MV/cm to 0.12 MV/cm. This optimization not only increases the breakdown voltage of the device but also reduces the high electric field strength near the gate. Consequently, it significantly reduces local Joule heat generation and improves the thermal reliability of the device.

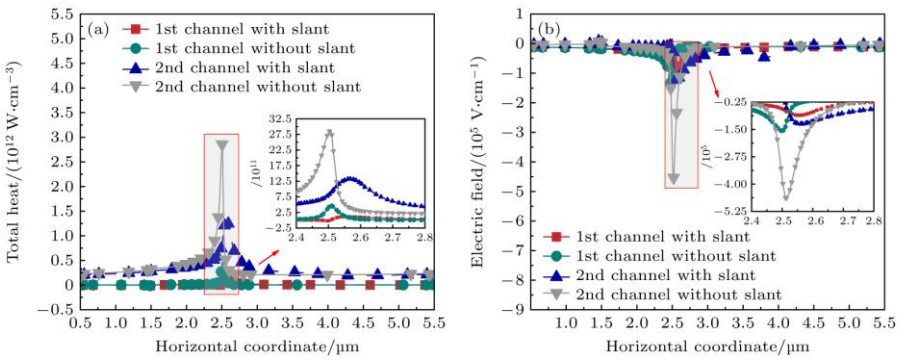


Fig. 10 V_{GS} = 0 V, V_{DS} = 10 V, Devices with two types of field plates, at 1 nm below the AlGaN/GaN interface: (a) Heat flux density distribution; (b) transverse electric field distribution.

3.3 Impact of Slanted Field Plate Structural Parameters on Device Performance

This section analyzes the influence of field plate length L_{FP} and tilt angle θ on device performance using a slanted field plate dual-channel GaN HEMT as an example. The goal is to optimize performance and enhance thermal reliability. Figure 11 illustrates the internal channel temperature distribution of devices with different L_{FP} and θ values under identical bias conditions (V_{GS} = 0 V, V_{DS} = 10 V). As shown in Figure 11(a), the maximum device temperature initially decreases and then increases with increasing θ, eventually stabilizing. The minimum maximum temperature occurs at $\theta = 6°$. When

$\theta \geqslant 8°$, the maximum temperature remains essentially stable. Based on this result, we further investigated the effect of L_{FP} on the maximum device temperature using $\theta = 6°$ as the baseline. The results are presented in Figure 11(b). The maximum device temperature changes significantly with variations in L_{FP}, reaching its lowest value at $L_{FP} = 1.2\mu m$. This phenomenon results from the combined effects of the slanted field plate structure and the passivation layer thickness. Changes in θ or L_{FP} of the slanted field plate alter the thickness of the underlying passivation layer, thereby affecting device performance. On one hand, the passivation layer thickness influences the modulation of charge distribution within the channel by the field plate. This subsequently affects the electric field and local heat flux density distribution. On the other hand, it impacts the internal heat conduction paths of the device. Under this electro-thermal coupling mechanism, the internal temperature distribution of the device changes significantly with adjustments to the field plate structural parameters.

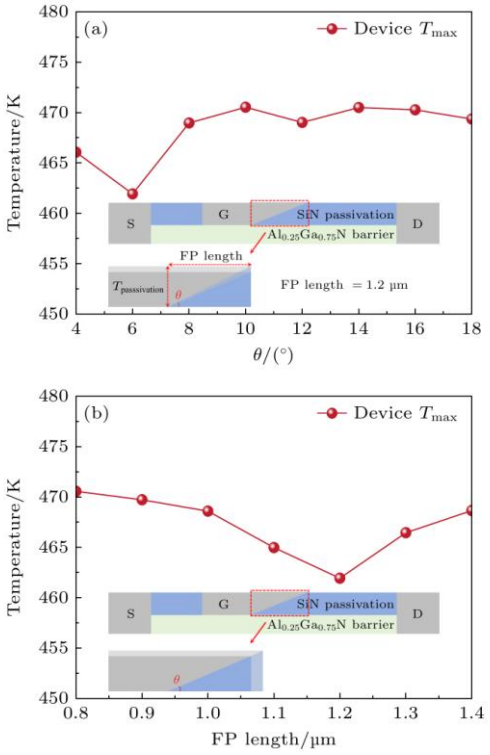


Fig. 11 Channel temperature of slanted field plate devices: (a) Different ϑ; (b) different L_{FP}.

Figure 12 presents the heat flux density and electric field distributions at a depth of 1 nm below the AlGaN/GaN interface for devices with seven different L_{FP} values under identical bias conditions (V_{GS} = 0 V, V_{DS} = 10 V). Since the slanted field plate exerts a more significant influence on the upper channel performance, the analysis primarily focuses on the upper channel. As observed in Figure 12(b), when $L_{FP} = 0.4\mu m$, the peak electric field intensity at the field plate edge exceeds that at the gate edge. This occurs because a shorter field plate fails to achieve uniform charge distribution, leading to

increased electric field intensity at its edge. As L_{FP} increases, the peak electric field intensities at both the gate and field plate edges gradually decrease, indicating a more uniform distribution of channel charge between the gate and drain. A comparison of Figure 12(a) and Figure 12(b) reveals close agreement in the variation trends between heat flux density and electric field distribution. This suggests that optimizing the electric field distribution via the field plate is an effective approach for reducing the peak heat flux density. However, when $L_{FP} \geqslant 1.2\mu m$, further increasing the length yields limited improvement in the peak electric field intensity at the gate edge and the peak heat flux density. This phenomenon is primarily attributed to two factors. First, as the field plate extends toward the drain, the thickness of the passivation layer beneath its terminal increases, thereby weakening its modulation capability on the channel potential[39]. Second, the field plate terminal approaches the drain too closely, significantly reducing the potential difference between the plate and the underlying channel, which diminishes the electric field modulation effect. Furthermore, an excessively long field plate exacerbates depletion region expansion, resulting in decreased saturation current and introducing additional parasitic capacitance. Meanwhile, the proximity of the field plate edge to the drain leads to increased electric field intensity in this region[38], potentially creating new hot spots and adversely affecting the thermal reliability of the device.

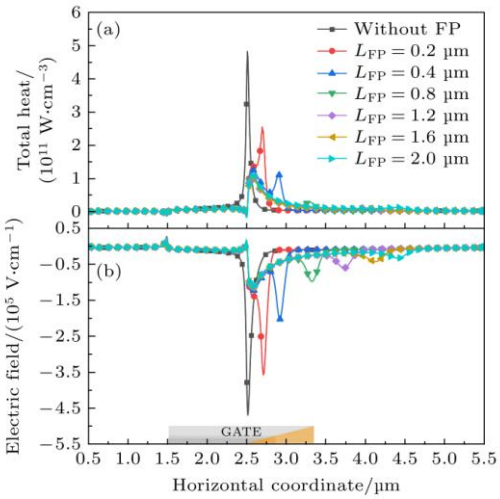


Fig. 12 Devices with different LFP values, (a) Heat flux density distribution at 1 nm below the upper AlGaN/GaN interface; (b) electric field distribution at 1 nm below the upper AlGaN/GaN interface.

The tilt angle θ is another critical parameter affecting the performance of tilted field-plate devices. Based on previous results, we investigated the impact of different tilt angles θ on device performance while fixing L_{FP} at 1.2 μm. Figures 13(a) and 13(b) present the heat flux density and electric field distributions 1 nm below the AlGaN/GaN interface, along with the output characteristics, for devices with six different θ values

under identical bias conditions (V_{GS} = 0 V, V_{DS} = 10 V). As θ decreases, the heat flux density and electric field distribution between the gate and drain become more uniform, leading to a reduction in the average internal temperature of the device. This improvement arises from two factors. First, a smaller θ corresponds to a thinner passivation layer, which improves heat dissipation from the device. Second, a smaller θ strengthens the ability of the field plate to modulate the underlying electric field, thereby optimizing the heat flux density distribution. When θ is large, the improvement in thermal reliability provided by the slanted field plate is limited. The primary reason is that the thicker passivation layer introduces higher thermal resistance, hindering heat dissipation. The results in Figure 13(c) indicate that the saturation current of the device does not change monotonically with θ. The decrease in saturation current at smaller θ values mainly stems from the risk of reduced breakdown voltage and current leakage due to the thinning of the passivation layer. Conversely, at larger θ values, the thickening of the passivation layer weakens the electric field modulation capability of the field plate, also leading to a decline in saturation current. Therefore, it is necessary to identify a geometric configuration that balances thermal reliability and electrical performance. For instance, when $\theta = 6°$ and L_{FP} = 1.2μm, the device maintains good thermal reliability without significant degradation in electrical performance.

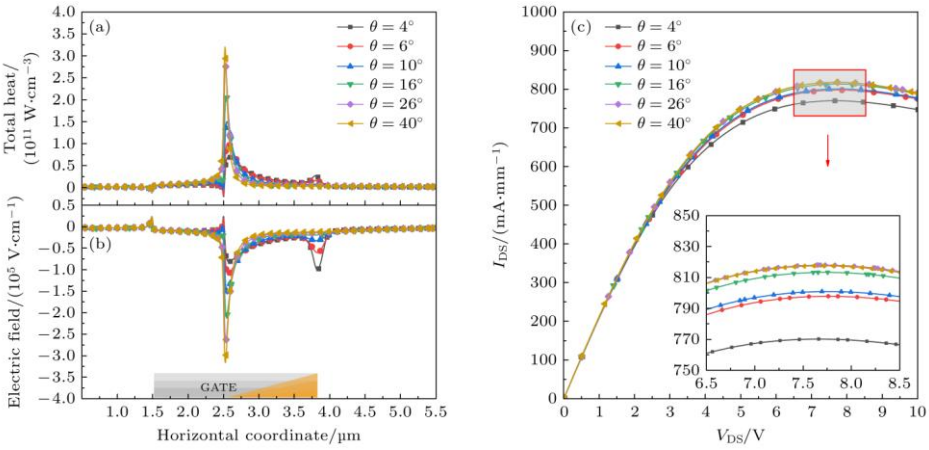


Fig. 13 Devices with different θ values, (a) Heat flux density distribution at 1 nm below the upper AlGaN/GaN interface; (b) electric field distribution at 1 nm below the upper AlGaN/GaN interface; (c) output characteristic curves.

Overall, the tilt angle θ of the slanted field plate primarily regulates the magnitude of the peak electric field intensity through a geometric smoothing effect. In contrast, the field plate length L_{FP} determines the spatial coverage of this modulation. Furthermore, this angle dictates the gradient of potential change along the channel direction. A smaller θ results in a gentler potential variation along the channel, which decomposes concentrated potential jumps into multiple gradual steps. Consequently, this directly reduces the maximum electric field intensity between the gate and drain. It further

diminishes the peak local heat flux density dominated by Joule heating. The field plate length must ensure that this smooth potential transition extends sufficiently to cover the high-electric-field region. The combined action of these parameters transforms the electric field distribution from a sharp single-peak profile into a smoother distribution. Correspondingly, the heat flux density shifts from being highly localized to being more uniformly distributed along the channel. This significantly improves thermal reliability while enhancing the device breakdown voltage.

Due to the reduction in peak electric field intensity, the slanted field plate structure can increase the breakdown voltage threshold of the device under identical conditions, thereby enhancing operational safety. It should be noted that the model in this study is based on the assumption of an ideal lattice. It does not account for leakage effects introduced by non-ideal factors such as surface states and buffer layer defects in actual devices. For GaN HEMT devices employing slanted field plates, the presence of leakage causes the breakdown location to deviate significantly from the ideal high-electric-field region determined by the field plate structure. The physical mechanism involves leakage paths, such as surface states or buffer layer defects, providing transport channels for carriers that are preferred over intrinsic bulk avalanche. Under high-voltage stress, current concentrates through these local weak regions. This leads to Joule heat accumulation and thermal runaway. Consequently, the actual breakdown point shifts from the optimized bulk high-field region to locations dominated by leakage. For instance, surface leakage may cause breakdown to occur at the edge of the drain metal. Buffer layer defects may cause breakdown at random defect clusters within the bulk. Although slanted field plates effectively regulate electric field distribution under ideal conditions, the breakdown location in actual devices is primarily dominated by material defects and process-induced leakage bottlenecks, rather than coinciding with the designed high-field region.

4 Conclusions and Future Work

4.1 Conclusions

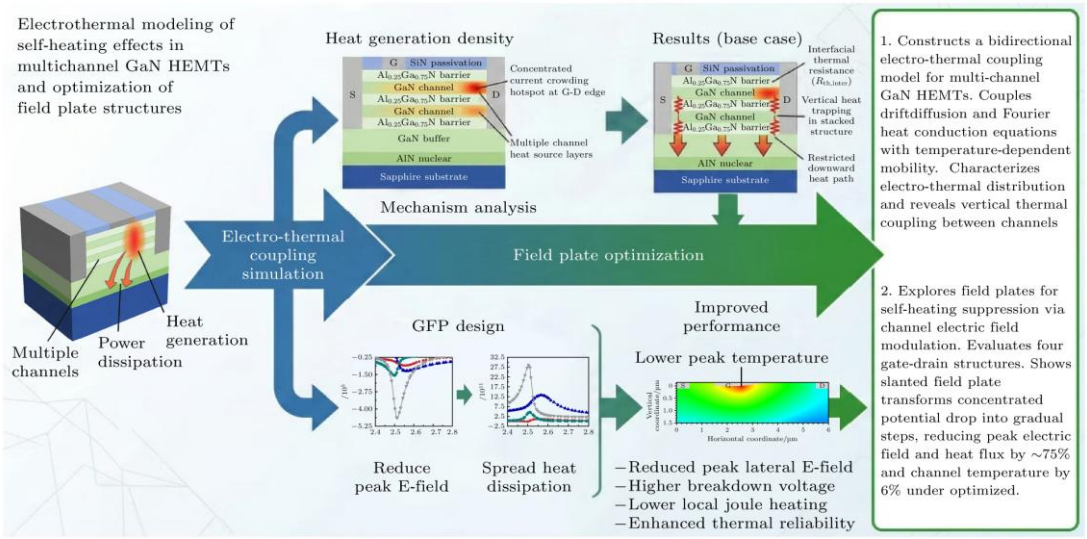
Based on the established electro-thermal bidirectional coupling model, this study systematically analyzed the electrical characteristics of GaN HEMT devices with different channel counts. These characteristics include band structure and output performance. The results indicate that the saturation current increases nonlinearly with the number of channels and eventually saturates. The primary reasons are the weakened control capability of the gate over distant channels and the reduction in carrier mobility caused by self-heating effects. To suppress self-heating effects, this study conducted dedicated simulations on the gate-drain field plate structure. The results demonstrate that the field plate structure effectively optimizes electric field distribution and

improves thermal characteristics. The slanted field plate yields the most significant improvement. By smoothing the channel electric field distribution, it reduces the peak channel temperature by approximately 4% compared to the structure without a field plate, assuming no significant difference in total power consumption. Through optimization of the geometric parameters (tilt angle and length) of the slanted field plate, the maximum electric field intensity and heat flux density are reduced by approximately 75% compared to the structure without a field plate. This is achieved with a tilt angle of 6° and a length of 1.2 μm. The peak channel temperature decreases from 472.8 K to 461.9 K, a reduction of approximately 6%, without adversely affecting the electrical performance of the device. In summary, an optimally designed slanted gate-drain field plate structure can significantly enhance the thermal reliability of multi-channel GaN HEMT devices. This provides effective technical support for improving their thermal stability and operational performance.

4.2 Future Work

In the study of high-power semiconductor devices, particularly multi-channel GaN HEMT devices, there is a strong interdependence between electrical performance and thermal reliability. Therefore, constructing an accurate electro-thermal bidirectional coupling model is crucial for precisely simulating the electrical and thermal behaviors of devices. Multi-channel GaN HEMT devices face the issue of weakened gate control over distant channels in practical applications. When extending the model from two-dimensional to three-dimensional, a partially surrounding gate structure could be introduced to enhance gate control over the channels. The impact of different gate structure parameters on device electrical performance and thermal reliability also requires systematic evaluation. It should be noted that the distribution of electric field and heat flux density in actual three-dimensional structures is far more complex than in two-dimensional models. It is not a simple extension of two-dimensional results, which demands greater modeling accuracy. The transition from two-dimensional to three-dimensional involves not only the complexity of governing equations and boundary conditions but also a significant increase in computational resource demands. Furthermore, as the feature size of GaN HEMT devices approaches the mean free path of phonons in GaN materials[39,40], the heat transport mechanism gradually transitions from diffusive to ballistic heat transport. The classical Fourier's law of heat conduction (Equation (9)) has limited applicability at this scale. Therefore, in subsequent research focusing on the spatially non-uniform distribution of heat flux density within three-dimensional devices, it is necessary to introduce non-Fourier heat conduction models. Examples include the single-phase-lag (SPL) model, the dual-phase-lag (DPL) model, and the phonon hydrodynamic equation. These models describe transient heat transport processes at the nanoscale. Additionally, combining transient heat conduction

analysis methods would provide a more realistic representation of the transient temperature rise and heat transport behavior of devices under pulse or high-frequency operating conditions. This provides theoretical guidance for failure assessment and thermal reliability design of devices under extreme conditions.



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