Wide bandgap high power electronic device junction temperature measurement technology*

ZHANG Jingwen[1], WANG Shuai[2, 3], SHI Shang[3], MA Mingyang[1], WANG Zexu[1], HAO Menglong[1, *]

1. School of Energy and Environment, Southeast University, Nanjing 210096, China

2. School of Electronic Science and Engineering, Nanjing University, Nanjing 210033, China

3. Nanjing Electronic Devices Institute, Nanjing 210016, China

Abstract—Wide-bandgap semiconductor power devices based on materials such as gallium nitride (GaN), silicon carbide (SiC), and gallium oxide (Ga_2O_3) have gained widespread adoption in power electronics and radio-frequency systems, owing to their high critical electric field, high power density, and superior high-frequency performance. However, under high power density operating conditions, power devices experience significant self-heating, which raises the junction temperature and consequently degrades both performance and reliability. Accurate extraction and measurement of the junction temperature are therefore essential for elucidating heat generation mechanisms, optimizing thermal management designs, and enabling reliable lifetime predictions. This article systematically reviews the mainstream techniques for junction temperature measurement in wide-bandgap semiconductor devices, categorized into three primary classes: electrical methods, physical contact methods, and optical methods. For electrical methods, the principles underlying temperature-sensitive parameters are introduced, along with their capability for online monitoring. These approaches are particularly well suited for real-time temperature assessment in packaged devices. For physical contact methods, the implementation and measurement principles of techniques such as scanning thermal microscopy and on-chip integrated temperature sensors are evaluated. For optical methods, the principles and application scenarios of non-contact temperature measurement techniques, including infrared thermography, micro-Raman spectroscopy, and thermoreflectance, are analyzed in detail. Finally, the review discusses key challenges currently confronting junction temperature measurements in wide-bandgap devices, including the characterization of ultrafast transient thermal processes, three-dimensional mapping of embedded thermal distributions, and mitigation of strong interference from multiphysics-coupled signals. Prospects for future development are also outlined, encompassing multi-technique fusion approaches, novel deep thermal characterization methods, and the emergence of

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quantum-precision temperature sensing technologies.

Keywords power devices; junction temperature measurement; thermal management

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1 Introduction

Wide-bandgap high-power electronic devices, represented by gallium nitride (GaN), silicon carbide (SiC), and gallium oxide (Ga_2O_3), exhibit significant performance advantages over first- and second-generation semiconductor devices in high-power, high-frequency, and high-voltage applications[1-3]. These advantages stem from their high breakdown electric fields, high carrier saturation velocities, and superior high-frequency and high-power-density characteristics. Consequently, their output power density can be several times to orders of magnitude higher than that of conventional Si-based devices. As a result, they are widely used in power electronics, communication equipment, and military technologies[4]. However, the extremely high output power density leads to a sharp increase in heat flux density within the device, particularly in key regions such as submicron-scale channels and junctions. This phenomenon causing severe self-heating and a substantial rise in junction temperature[5]. Junction temperature is critical to both device performance and reliability. First, excessive junction temperature intensifies carrier scattering, reduces mobility, and increases on-resistance, thereby degrading electrical performance[6]. Second, every 10-15 ℃ increase in junction temperature doubles the device failure rate, serving as a core factor that significantly reduces the mean time between failures. Finally, junction temperature acts as a core parameter in models characterizing device health status and predicting lifespan[7]. Therefore, developing junction temperature measurement techniques with high precision and high spatiotemporal resolution has become a fundamental prerequisite for realizing the full performance potential of wide-bandgap semiconductor devices and ensuring their long-term reliable operation[8].

However, achieving precise junction temperature measurement for wide-bandgap semiconductor devices faces unprecedented technical challenges, primarily arising from the extreme operating conditions and unique physical structures of these devices[9]. On one hand, these devices often operate under extreme conditions characterized by high power density, high junction temperature (often exceeding 200 ℃), and high voltage. These conditions impose stringent requirements on the environmental adaptability, electrical insulation, and thermal stability of measurement sensors[10]. A

more fundamental challenge is the trade-off between measurement accuracy and spatiotemporal resolution. During high-frequency and high-voltage switching processes, channel temperature can fluctuate drastically on microsecond or even nanosecond timescales. This necessitates measurement techniques with extremely high temporal resolution to capture transient thermal characteristics[11]. Simultaneously, the scale of key heat-generating regions in devices is often at the submicron or even nanometer level, imposing strict requirements on the spatial resolution of measurement techniques.

For wide-bandgap high-power semiconductor devices, as shown in Figure 1, junction temperature measurement methods can be categorized into electrical methods, physical contact methods, and optical methods.

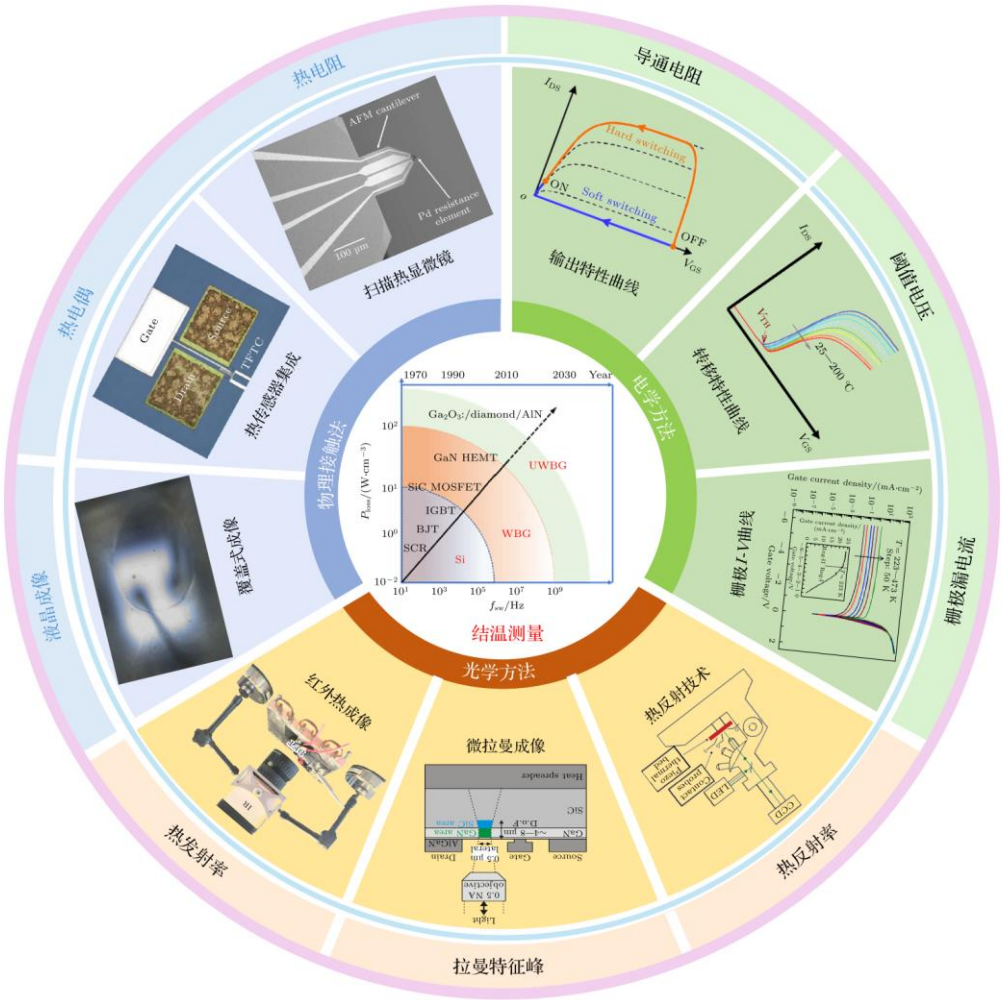


Fig. 1 Junction temperature measurement technology for wide-bandgap high-power electronic devices.

Electrical methods constitute a class of techniques that indirectly estimate junction temperature by measuring electrical parameters highly correlated with temperature. The core principle involves utilizing the device's inherent electrical characteristics,

known as temperature-sensitive parameters (TSPs), as built-in "temperature sensors." Common TSPs include on-resistance and threshold voltage[12–14]. Physical contact methods determine device temperature indirectly by measuring the temperature of an object or material in direct thermal contact with the device under test. Common techniques include scanning thermal microscopy and integrated sensors[15–17]. Optical methods are non-contact measurement techniques based on the principle of light-matter interaction. They infer junction temperature by detecting optical signal changes induced by temperature variations. Representative technologies include infrared thermography, micro-Raman spectroscopy, and thermoreflectance imaging[18,19].

Electrical, physical contact, and optical methods serve as common and practical approaches for evaluating the junction temperature of wide-bandgap high-power semiconductor devices. These methods provide critical support for characterizing device thermal properties. This paper aims to comprehensively review these three mainstream junction temperature measurement methods. Section 2 focuses on electrical methods, detailing the calibration mechanisms of TSPs and evaluating the applicability and limitations of different electrical parameters. Section 3 discusses physical contact methods, exploring their technical classifications, working principles, and application characteristics based on direct contact temperature measurement. It also assesses the advantages and disadvantages of various techniques regarding spatial resolution, measurement accuracy, and applicable scenarios. Section 4 systematically reviews optical methods, emphasizing the basic principles, system configurations, junction temperature testing procedures, and achievable temporal and spatial resolutions of infrared thermography, micro-Raman spectroscopy, and thermoreflectance. Finally, Section 5 discusses the core challenges facing junction temperature measurement for wide-bandgap high-power semiconductor devices and outlines opportunities brought by future technological developments.

2 Electrical Methods

In electrical temperature measurement research for wide-bandgap semiconductor devices, analysis methods must be distinguished according to device structure types. For devices such as GaN high electron mobility transistors (GaN HEMTs), SiC metal-oxide-semiconductor field-effect transistors (SiC MOSFETs), and Ga_2O_3 MOSFETs, output and transfer characteristic curves are crucial analysis tools[20]. The output characteristic curve illustrates the relationship between drain-source current (I_{DS}) and drain-source voltage (V_{DS}) at a fixed gate-source voltage (V_{GS}). This curve reflects TSPs such as on-resistance (R_{on}) and saturation drain current (I_{DSS}). The transfer characteristic curve describes the variation of I_{DS} with V_{GS} at a fixed V_{DS}. TSPs such as threshold voltage (V_{Th}) and transconductance (g_m) can be directly extracted

from this curve.

For power devices represented by GaN, SiC, and Ga_2O_3 Schottky barrier diodes (SBDs), the forward *I–V* characteristic curve is the core analysis method. Therefore, this section systematically reviews electrical measurement methods based on TSPs, categorized by device type. Additionally, this section explores other electrical temperature measurement methods that do not directly rely on *I–V* curves. These include methods based on TSPs such as gate leakage current (I_{GLeak}), gate resistance, and turn-on and turn-off times.

2.1 Calibration and Measurement

Typically, measuring the temperature of wide-bandgap semiconductor devices using electrical methods involves two basic steps: calibration and actual measurement[21]. The calibration phase aims to establish a stable functional relationship between TSPs and junction temperature. During this process, the device is placed in an external temperature control system, such as a high-precision thermal chamber or a temperature-controlled heatsink, to stabilize its temperature. Subsequently, the variation of TSPs with temperature is measured under specified electrical conditions. To ensure calibration accuracy, the self-heating effect caused by the measurement power (P_m) must be negligible. Therefore, extremely low P_m values are usually selected. If higher P_m is unavoidable due to parameter characteristics, the measurement time should be minimized to suppress errors introduced by self-heating.

The actual measurement phase applies the calibrated relationship between TSPs and temperature to real-world operating scenarios of the device. Based on differences in measurement timing and power control methods, mainstream approaches are classified into heating curve and cooling curve methods[22]. The heating curve method directly monitors the device's temperature rise response while applying heating power (P_D), as shown in Fig. 2(a). However, since this method continuously applies high power during measurement, it exacerbates trap effects and current collapse in devices such as GaN HEMTs. It may also cause defect-related electrical instability in Ga_2O_3 devices[23]. These effects distort the relationship between TSPs and temperature, thereby introducing significant measurement errors.

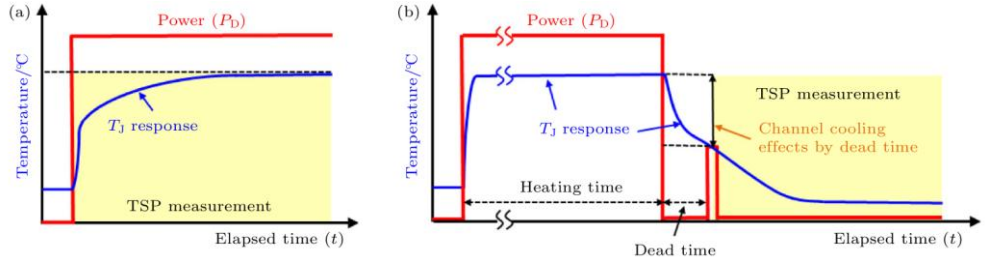


Fig. 2 Electrical temperature measurement methods[22]: (a) Heating curve technique; (b) cooling

The cooling curve method first brings the device to thermal steady state under heating power. It then switches the heating power to a measurement power and records the temperature decay process, as shown in Fig. 2(b). However, this method is affected by the propagation delay of electrical switching control signals and the turn-on/turn-off times of the switching devices themselves. Although the delay time is typically on the order of milliseconds or microseconds, its impact cannot be ignored for transient thermal tests that need to capture the initial cooling process within the first few microseconds or even nanoseconds[24]. Furthermore, at the instant when the high current is cut off, parasitic inductance and capacitance in the test fixture and circuit board traces induce strong voltage and current oscillations. These oscillations may completely overwhelm the weak electrical signals reflecting the junction temperature. If measurements are taken during this period, the acquired data will consist primarily of noise. Therefore, data acquisition must wait until the oscillations have sufficiently decayed and the circuit has stabilized. This waiting period constitutes the "dead time" in the measurement, which is particularly pronounced for GaN HEMTs with extremely fast switching speeds and SiC devices operating at high voltages and large currents. Consequently, extrapolation is often required to infer the junction temperature at the instant of power cutoff.

2.2 On-state Resistance

When a semiconductor device is in the on-state, with a forward bias applied between the gate and source, and operates in the linear region, the on-state resistance R_{on} characterizes the overall resistance of the conductive path from drain to source. From the perspective of carrier transport mechanisms, R_{on} typically exhibits a significant positive temperature coefficient, meaning it increases as the junction temperature rises. The primary physical mechanism is that increased temperature enhances phonon scattering and reduces electron mobility, thereby increasing the device resistance. Based on this principle, Qin et al.[8] calibrated the monotonic relationship between the R_{on} of GaN HEMTs and junction temperature under low-voltage conditions (Fig. 3(a)). In actual measurements, they calculated R_{on} in real time using the on-state V_{DS} and I_{DS} to infer the junction temperature. This method yielded an average measurement error of less than 10% within a 100 ℃ range when comparing the predicted junction temperature with the actual junction temperature of GaN HEMTs measured by infrared thermography (Fig. 3(b)), thus validating the effectiveness of this temperature measurement method. Li et al.[25] designed a dual pulse test (DPT) circuit. By introducing an additional phase leg, they effectively eliminated the influence of pre-bias voltage stress in the off-state of GaN HEMTs, thereby achieving a more

accurate evaluation of R_{on} as a temperature-sensitive electrical parameter. The results indicated that under low-voltage conditions, the device R_{on} exhibits good linear temperature characteristics, increasing steadily with rising temperature.

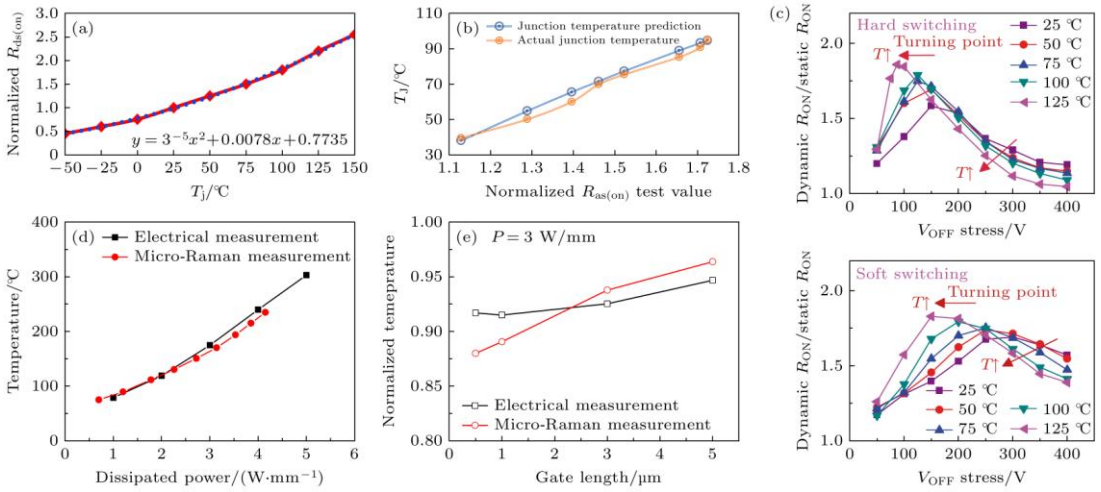


Fig. 3 (a) Relationship between the normalized R_{on} and junction temperature of GaN HEMT[8]; (b) online junction temperature prediction results[8]; (c) dependence of dynamic R_{on}, normalized to the corresponding static R_{on}, on V_{OFF} stress across temperatures under hard and soft switching; (d) comparison between electrical measurement and Raman measurement at different power dissipation levels[30]; (e) normalized temperature profile relative to the gate length[30].

However, under high-voltage stress and actual switching conditions, the variation in R_{on} is not determined solely by temperature. It is also significantly influenced by electron trapping effects induced by strong electric fields and current collapse effects. These factors collectively result in exceptionally complex variations in the dynamic R_{on} of GaN HEMTs[26,27]. For instance, Li et al.[28] used double pulse testing (DPT) and multi-pulse testing (MPT) to demonstrate that the static R_{on} of GaN HEMTs increases monotonically with temperature. At 150 ℃, it is approximately 2.46 times the value at 25 ℃. However, the authors also noted significant "dynamic R_{on} degradation" during actual switching processes. This phenomenon manifests as resistance values measured during switching that are far higher than static values. In DPT or single-pulse tests, high temperatures may mitigate the trend of R_{on} degradation. Yet, in MPT scenarios that more closely resemble practical applications (characterized by high frequency and multiple pulses), high temperatures synergize with high voltage and large currents. This synergy causes a sharp increase in dynamic R_{on} degradation. Li et al.[29] conducted an in-depth study on the temperature characteristics of dynamic R_{on} in hybrid drain-embedded gate injection transistors (HD-GIT). They focused on the variation of R_{on} with temperature under hard and soft switching conditions. The results indicated that dynamic R_{on} exhibits significant temperature dependence and is

closely related to switching conditions. As shown in Fig. 3(c), the normalized dynamic R_{on} (relative to the static R_{on} at each temperature point) displays distinct non-monotonic characteristics with respect to off-state voltage (V_{OFF}) stress under both hard and soft switching conditions. At high temperatures (125 ℃), the peak of dynamic R_{on} occurs at lower V_{OFF} stress levels. Furthermore, the turning point voltage under hard switching is significantly lower than that under soft switching. This suggests that high temperatures help improve dynamic conduction characteristics.

Additionally, Wu et al.[30] proposed an electrical thermometry method for GaN HEMT structures with multiple gate lengths. This method measures the channel temperature beneath the gate by extracting the temperature-dependent channel sheet resistance (R_{ch}). Specifically, R_{ch} is precisely isolated using the equation $\Delta R_{on}(T) = R_{ch}(T)\cdot\Delta L_G/\Delta W_G$, where L_G and W_G represent the gate length and gate width, respectively. As illustrated in Fig. 3(d), the temperature trends measured by this method align closely with those obtained via Raman thermometry within a power density range of 0—5 W/mm. Further analysis normalized by gate length (Fig. 3(e)) revealed that the electrical method offers significant advantages for short-gate devices. This advantage stems from the higher sensitivity of channel resistance thermometry to the temperature of the channel region beneath the gate. In contrast, the spatial resolution of Raman thermometry is limited by the mutual interference between the laser spot size and the gate geometry. However, the authors also pointed out that current collapse effects in the electrical method introduce measurement uncertainty.

Similar to GaN HEMTs, the R_{on} of SiC MOSFETs exhibits significant dependence on junction temperature. Zhang and Liang[31] monitored the junction temperature of SiC MOSFETs in real time based on R_{on}. They established a linear relationship between R_{on} and junction temperature (Fig. 4(a)), expressed as $R_{on} = p\cdot T_j + q$. Experimental calibration yielded $p = 0.54$ mΩ/℃ and $q = 61$ mΩ. Stella et al.[32] similarly developed a linear model for the variation of R_{on} with the junction temperature of SiC MOSFETs. Experiments showed that as the junction temperature increased from 25 ℃ to 145 ℃, the R_{on} of the SiC MOSFET increased by 84%, with a sensitivity of 0.54 mΩ/℃. For Ga_2O_3 MOSFETs, Ren et al.[33] investigated the temperature characteristics of their R_{on}. They first recorded the transfer characteristic curves of Ga_2O_3 MOSFETs using a semiconductor analyzer (Fig. 4(b)) and extracted R_{on} from these curves. As shown in Fig. 4(c), R_{on} increased from 222 Ω·mm at 50 ℃ to 299 Ω·mm at 298 ℃, exhibiting a positive temperature coefficient. This study confirmed that R_{on} can serve as a sensitive parameter for junction temperature measurement. However, the activation of interface traps at high temperatures may cause non-linear changes in the resistance-temperature relationship. Therefore, temperature calibration is required to ensure measurement accuracy.

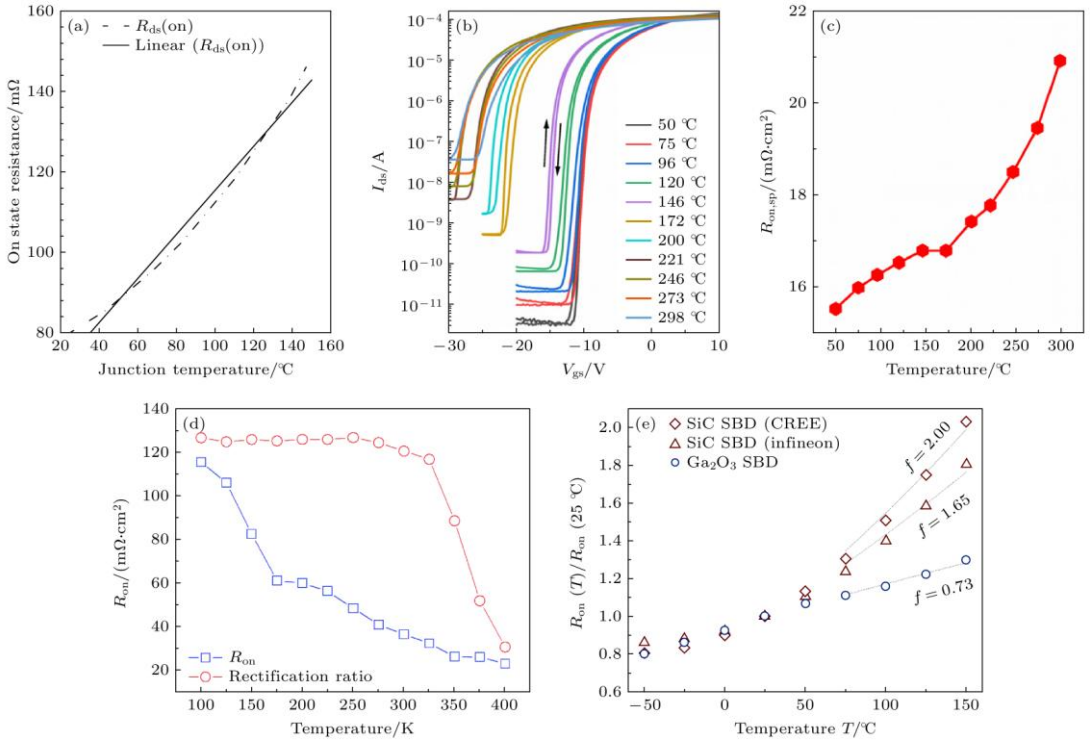


Fig. 4 (a) Relationship between R_{on} and junction temperature of SiC MOSFET[31]; (b) transfer characteristic curve of Ga_2O_3 MOSFET[33]; (c) relationship between R_{on} and junction temperature of Ga_2O_3 MOSFET[33]; (d) temperature dependence of R_{on} in Ga_2O_3 SBD[34]; (e) R_{on} of two commercial SiC SBDs and the Ga_2O_3 SBD at different temperatures, normalized to the respective R_{on} at 25 ℃[35].

Regarding SBD devices, Reddy et al.[34] demonstrated that the R_{on} of Ga_2O_3 SBDs exhibits a significant decreasing trend with increasing temperature, as shown in Fig. 4(d). This negative temperature coefficient arises because carrier mobility decreases with rising temperature, which tends to increase resistance. However, the concentration of free carriers generated by thermal excitation increases significantly, ultimately causing the on-resistance to decrease as temperature rises. Wilhelmi et al.[35] compared the temperature dependence of normalized on-resistance between commercial SiC SBDs and Ga_2O_3 SBDs (Fig. 4(e)). They found that the thermal coefficient f of Ga_2O_3 devices is only 0.73, which is significantly lower than that of SiC devices (1.65—2.00). This indicates that the on-resistance of Ga_2O_3 devices varies more gently with temperature.

2.3 Saturation Drain Current

When V_{DS} exceeds a certain threshold, I_{DS} enters the saturation region, where it should ideally remain constant. In practice, however, self-heating effects significantly influence device characteristics in the saturation region[36-38]. On one hand, carrier mobility decreases with increasing temperature, causing the saturation current to drop as temperature rises. On the other hand, within the saturation region, especially in

devices with small dimensions and high current densities, self-heating causes the channel temperature to rise continuously. This leads to a further decrease in mobility, manifesting as a reduction in I_{DS} with increasing V_{DS}, as illustrated in Fig. 5(a). To quantify this effect, Zhang et al.[36] established a linear relationship between I_{DSS} and temperature for GaN HEMTs. They clearly revealed that I_{DSS} decreases linearly with increasing temperature and calculated a temperature coefficient α of -0.077 mA/K. McAlister et al.[39] further correlated the I_{DS} of GaN HEMTs with power dissipation (Fig. 5(b)). Using this method, they quantitatively compared the thermal performance of different substrate materials. They found that under the same power conditions, the channel temperature rise in GaN HEMTs on sapphire substrates can be 2.7 times that of devices on SiC substrates. Marin et al.[40] systematically confirmed and expanded upon this direction. By measuring the variation in I_{DS} for GaN HEMTs grown on SiC, Si, and sapphire substrates over the range of 0—225 ℃, and using the difference in I_{DS} between DC ($I_{D.DC}$) and pulsed ($I_{D.Pulsed}$) conditions (Fig. 5(c)) combined with the temperature sensitivity coefficient θ, they achieved precise calculation of the channel temperature ($T_{channel} = T_{amb}+(I_{D.DC}-I_{D.Pulsed})/\theta$). Fig. 5(d) shows the relationship between channel temperature and power density at different ambient temperatures. The results indicate significant differences in self-heating behavior among devices fabricated on different substrates, confirming that the substrate plays a key role in the self-heating process.

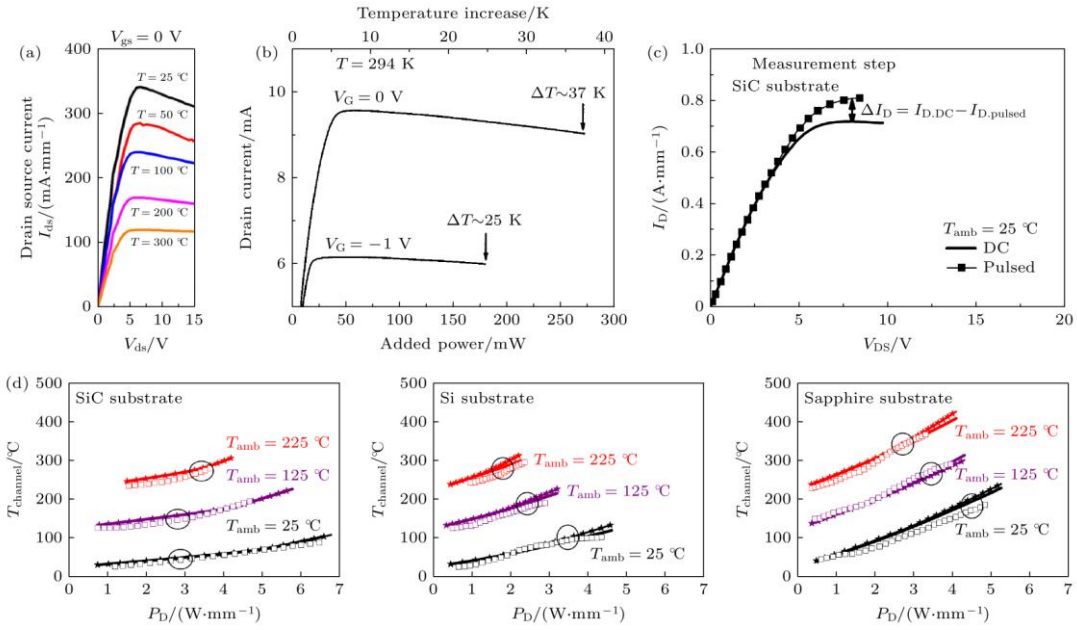


Fig. 5 (a) I_{DS}-V_{DS} characteristics at different temperatures[37]; (b) the relationship between drain current and applied power as well as temperature rise[39]; (c) I_{DS}-V_{DS} characteristics under DC ($I_{D.DC}$) and pulsed ($I_{D.Pulsed}$) conditions[40]; (d) channel temperature versus power density for devices grown on SiC, Si, and sapphire substrates[40].

Device structure innovation provides a new approach to suppressing current degradation caused by self-heating effects. Tamura et al.[38] fabricated a multi-mesa channel (MMC) GaN HEMT, with the device structure shown in Fig. 6(a). By comparing the transfer characteristics of conventional planar HEMTs and MMC HEMTs (Fig. 6(b)) at different temperatures, it is clearly observed that the drain current of the MMC structure exhibits nearly temperature-independent behavior over a wide temperature range of 120—500 K. The authors attribute this phenomenon to the effective modulation of the channel potential distribution by the surrounding gate structure of the MMC, thereby forming an enhanced electric field confinement effect around the two-dimensional electron gas.

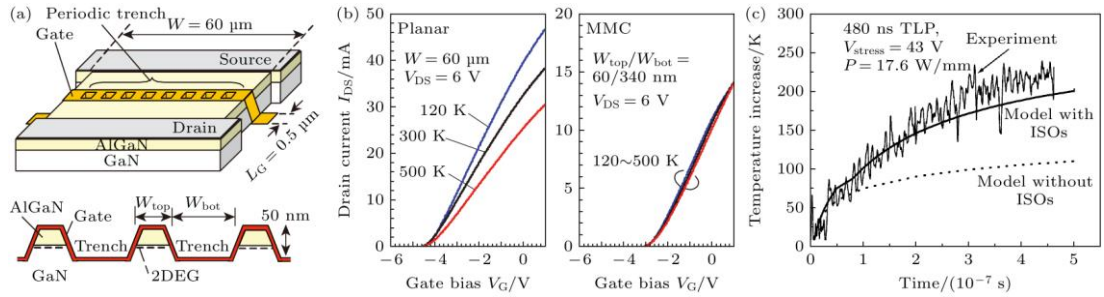


Fig. 6 (a) Schematic illustration of the MMC GaN HEMT[38]; (b) temperature dependence of the transfer characteristics for planar and MMC GaN HEMTs[38]; (c) comparison between experimental and calculated transient temperature rise after a 480 ns pulse[42].

Although the aforementioned analysis methods based on steady-state or quasi-steady-state current provide an effective basis for evaluating device thermal characteristics, GaN HEMTs often operate in pulsed modes in practical power switching or radio frequency applications. The resulting temperature fluctuations, occurring on microsecond to nanosecond timescales, are difficult to capture using steady-state analysis[41]. Therefore, conducting transient thermal characteristic research is essential for achieving real-time, dynamic monitoring of channel temperature. Kuzmłk et al.[42] developed a GaN HEMT channel temperature extraction technique based on I_{DS} transient decay. They employed transmission line pulses with a width of 480 ns to synchronously acquire I_{DS} and voltage waveforms. They observed that the magnitude of I_{DS} decay was positively correlated with pulse power dissipation. By utilizing the temperature dependence of source resistance calibrated via steady-state heating from 25 to 250 ℃, and iteratively solving the expression $\Delta I_{DS} = -g_m I_{DS} \Delta R_S(T)$, they successfully reconstructed the transient variation of channel temperature (Fig. 6(c)). This achievement extended the current method from steady-state to transient applications.

Regarding SiC MOSFETs, Yang et al.[43] inserted two test voltage levels (V_{GS1} = 3.86 V,

V_{GS2} = 4.68 V) during the turn-on process of SiC MOSFETs to collect the corresponding saturation currents I_{D1} and I_{D2}. The results indicated that the square roots of these two I_{DSS} values exhibited a highly linear relationship with temperature (Fig. 7(a), (b)). The sensitivity of I_{D1} was 0.15 mA/℃$^{1/2}$, while that of I_{D2} was 0.18 mA/℃$^{1/2}$. Du et al.[44] controlled the temperature of SiC MOSFETs (25-145 ℃) using a heating plate in a double-pulse test circuit. They used an oscilloscope to acquire I_{DS} waveforms under different load currents (7-11 A). Figure 7(c) displays only the waveform for a current of 7 A. Their study revealed that I_{DS} increased significantly with rising temperature during the current rise phase. For Ga_2O_3 MOSFETs, Zheng et al.[45] designed a four-stage measurement sequence including pre-trapping, as shown in Fig. 7(d). This approach effectively suppressed the interference of trap effects on I_{DS} temperature measurements in Ga_2O_3 MOSFETs. However, since this method measures the average temperature between the source and drain, it exhibited a 27% discrepancy compared to the peak temperature obtained from three-dimensional thermal simulations (Fig. 7(e)). Wong et al.[46] leveraged the temperature sensitivity of I_{DS}. By extracting the I_{DS} decay caused by self-heating under DC conditions, they inverted the data to determine the actual channel temperature of Ga_2O_3 MOSFETs (Fig. 7(f)).

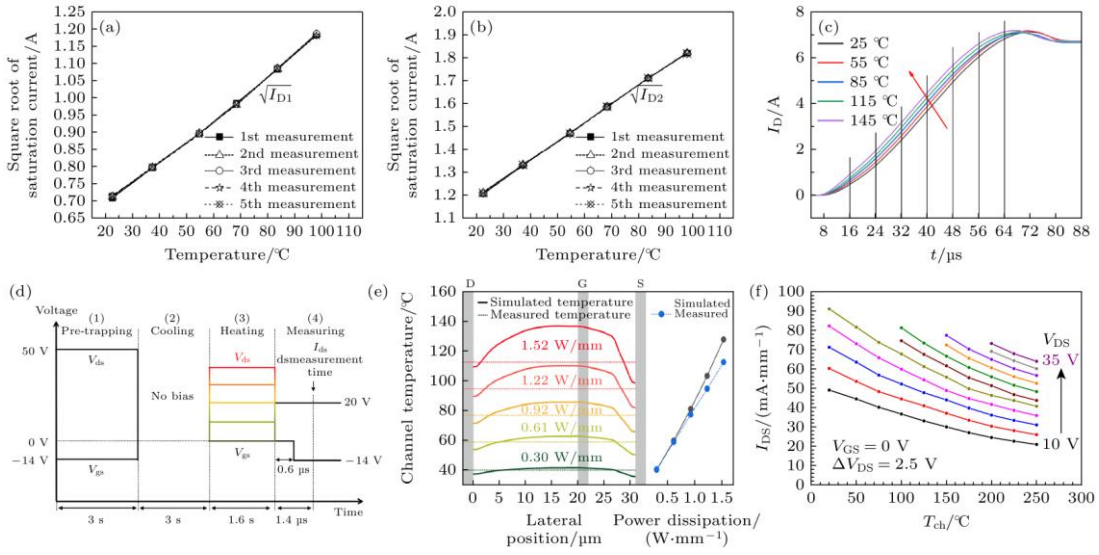


Fig. 7 (a) Relationship between the square root of I_{D1} and (b) I_{D2} of the SiC MOSFET and the junction temperature[43]; (c) I_{DS} at different temperatures with a load current of 7 A[44]; (d) four-stage method for measuring the junction temperature of Ga_2O_3 MOSFETs[45]; (e) comparison between simulated channel temperature profiles and measured temperatures[45]; (f) variation of I_{DS} with the channel temperature of the Ga_2O_3 MOSFET at different V_{DS} values[46].

2.4 Threshold Voltage

V_{Th} is defined as the voltage applied across the gate and source terminals of a semiconductor device when a specified current flows through the drain at ambient temperature. Typically, the specified I_{DS} falls within the microampere or milliampere range[47,48]. Based on this definition, Sharma et al.[49] systematically evaluated the temperature dependence of V_{Th} in GaN HEMTs using both static and dynamic methods. In static measurements, the V_{Th} extracted via the constant current criterion (with a threshold current of 2.6 mA) exhibited a strong linear negative temperature dependence, as shown in Fig. 8(a) and (b), with a sensitivity of -0.84 mV/K. Dynamic measurements utilized the parasitic inductance between the power source and the Kelvin source (*V*ss') as a trigger signal. When *V*ss' exceeded a set reference voltage, the data acquisition circuit precisely captured the gate-source voltage at that instant, defining it as the quasi-threshold voltage. This approach effectively prevented false triggering and noise interference, as illustrated in Fig. 8(c) and (d), achieving a measured sensitivity of -2.5 mV/K.

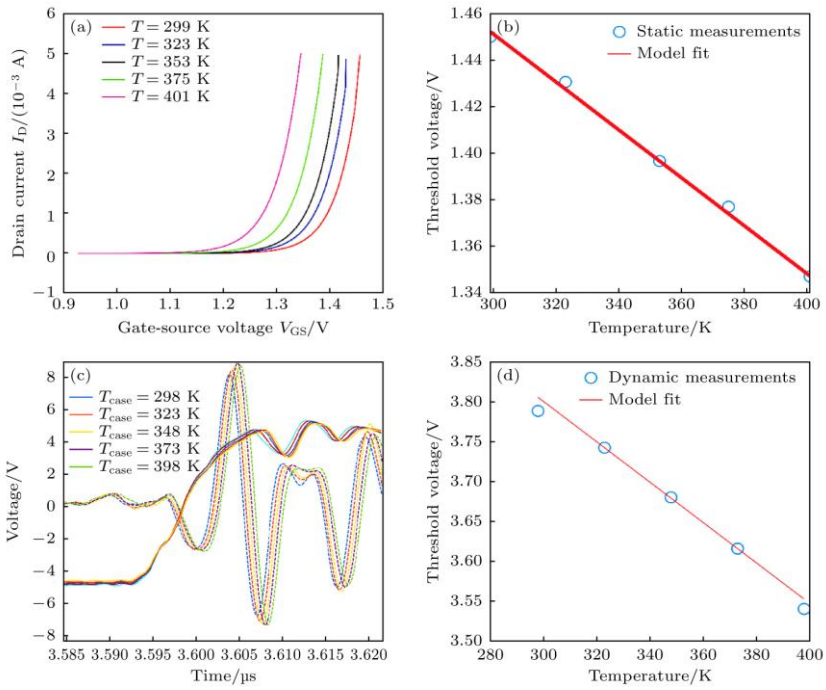


Fig. 8 (a) I_{DS}-V_{GS} transfer characteristic curve[49]; (b) static measurement[49]; (c) turn-on transient curve of GaN HEMT (V_{DS} = 400 V, I_{DS} = 4 A)[49]; (d) dynamic measurement[49].

However, subsequent studies have revealed that the temperature-dependent behavior of V_{Th} in GaN HEMTs is far from a simple linear relationship. The drift direction (positive or negative) and variation pattern depend heavily on the specific device structure and operating conditions. The study of p-GaN HEMTs by Chae et al.[50] illustrates this complexity. As shown in Fig. 9(a), at a low gate voltage (2 V), the V_{Th}

shift exhibits a unique reversal phenomenon with increasing temperature: it shows a positive shift with decreasing magnitude in the 25—75 ℃ range, and transitions to a negative shift with increasing magnitude above 75 ℃. This reversal is attributed to the competition between electron trapping and hole injection mechanisms in different temperature ranges. In contrast, at a high gate voltage (8 V), although the V_{Th} shift remains negative, its magnitude decreases above 100 ℃, suggesting that the dominant mechanism may shift to hole detrapping at high temperatures (Fig. 9(b)). These findings demonstrate that the operating point (gate voltage) is a key variable influencing the temperature characteristics of V_{Th}.

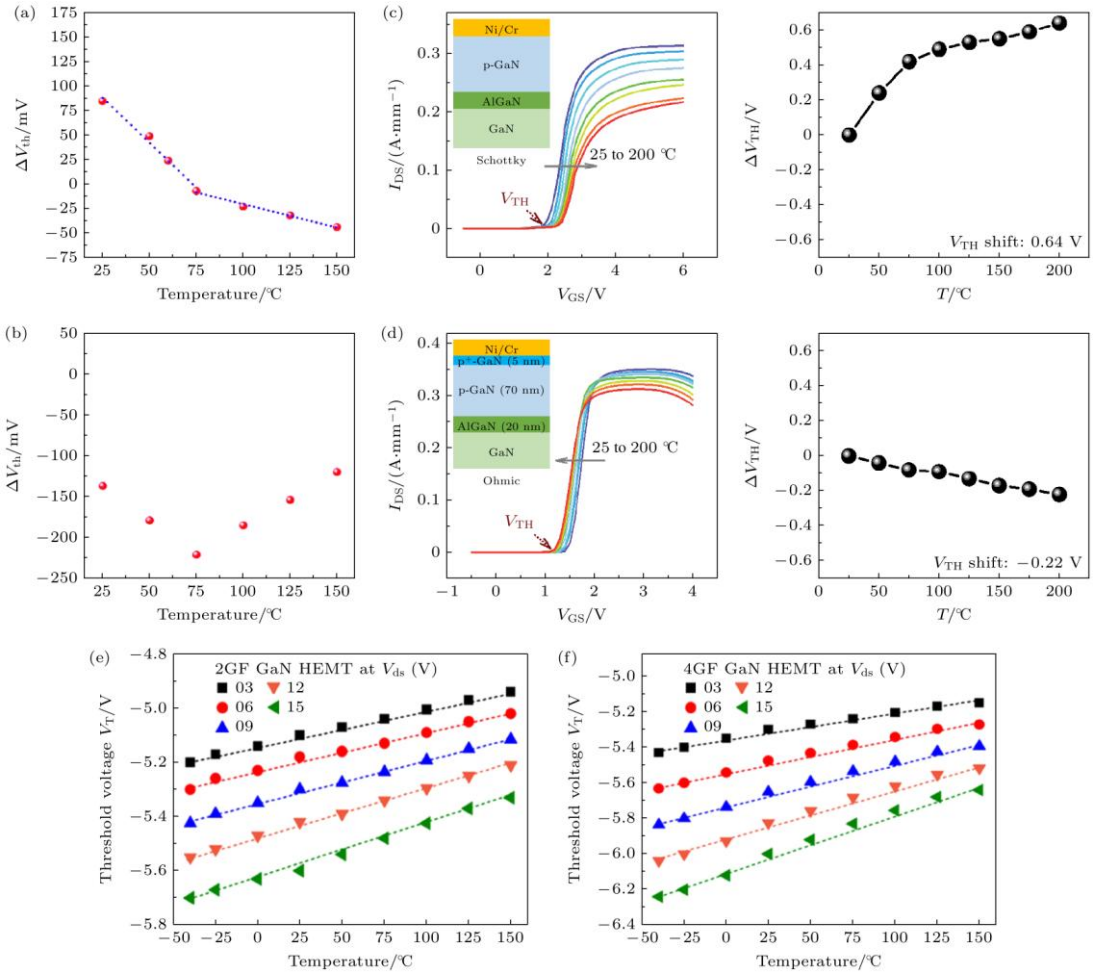


Fig. 9 V_{Th} versus temperature at gate biases of (a) 2 V and (b) 8 V[50]; transfer characteristics of the (c) Schottky-type device and (d) the ohmic-type device in the temperature range of 25 ℃ to 200 ℃, the insets illustrate the gate structures of the Schottky-type and ohmic-type devices, respectively[51]; V_{Th} as a function of temperature and V_{DS} for (e) 2GF and (f) 4GF GaN HEMTs[48].

In addition to operating conditions, the gate structure type is a fundamental factor determining the direction of V_{Th} drift in GaN HEMTs. Wang et al.[51] found that GaN HEMTs with Schottky gate structures and those with ohmic gate structures exhibit opposite V_{Th} temperature characteristics, as shown in Fig. 9(c) and (d). This difference

stems from distinct internal voltage distribution mechanisms. For ohmic-gate devices, V_{Th} decreases with increasing temperature, showing negative drift. This behavior is primarily caused by the "knee voltage" (V_{Knee}) in their current characteristics. This voltage consumes part of the external gate bias, and its value drops significantly as temperature rises, thereby reducing the effective voltage required to turn on the device[52]. In contrast, V_{Th} in Schottky-gate devices increases with temperature, exhibiting positive drift. This occurs because the metal-semiconductor junction shares part of the voltage. As temperature rises, the voltage drop across this junction increases. To maintain the effective turn-on voltage across the PN junction, a higher external gate bias is required, resulting in positive V_{Th} drift. Furthermore, Alim et al.[48] observed a positive drift trend in GaN HEMTs with two different gate finger structures (2GF and 4GF), as illustrated in Fig. 9(e) and (f). They attributed this mainly to the temperature-dependent variation in Schottky barrier height. The V_{Th} of the 2GF device was -5.6 V at 25 ℃, while that of the 4GF device was -6.0 V, indicating that short-channel devices exhibit more negative V_{Th} characteristics.

Furthermore, internal band structure design and interface engineering critically influence the thermal stability of V_{Th} in GaN HEMTs. Yang et al.[53] investigated the relationship between V_{Th} and junction temperature in two structures: GaN metal-insulator-semiconductor HEMTs (MIS-HEMTs) and metal-oxide-semiconductor channel HEMTs (MOSC-HEMTs). The schematic structures of these devices are shown in Fig. 10(a). Experimental results indicate that, unlike MOSC-HEMTs whose V_{Th} remains nearly constant with temperature, MIS-HEMTs exhibit significant negative V_{Th} drift (Fig. 10(b)), even when employing high-quality gate dielectric/GaN interfaces. The underlying cause is the presence of a polarization barrier layer in MIS-HEMTs. This layer spatially isolates the critical gate dielectric/GaN interface from the channel, thereby raising the energy bands at the interface. Consequently, interface trap levels located "deeper" above the Fermi level can move more freely in the pinch-off state, leading to a pronounced negative shift in V_{Th} with temperature.

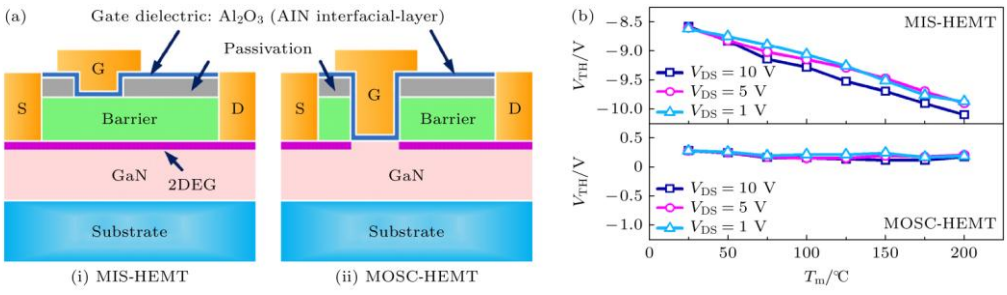


Fig. 10 (a) Cross-sectional schematic diagrams of MIS-HEMT and MOSC-HEMT; (b) temperature dependence of threshold voltage for MIS-HEMT and MOSC-HEMT at V_{DS} of 1 V, 5 V, and 10 V[53].

For SiC MOSFETs, Yu et al.[54] analyzed the turn-on transient process. They utilized the parasitic inductance jump between the power source and the Kelvin source to precisely capture the conduction critical point. This approach converted the temperature dependence of V_{Th} into a measurable time parameter. The study revealed a linear negative correlation between the quasi-threshold voltage and junction temperature under different load currents (Fig. 11(a)). The sensitivity reached -4.37 mV/℃. Based on the same principle, Jiang et al.[55] validated SiC MOSFETs under different source-drain voltages. As shown in Fig. 11(b), the dynamic V_{Th} exhibits a strong negative linear relationship with junction temperature. The temperature sensitivity reaches -5.2 mV/℃. Regarding Ga_2O_3 MOSFETs, Ren et al.[33] measured the transfer characteristic curves via bidirectional scanning within the temperature range of 50-298 ℃. They observed a significant negative drift in V_{Th} as temperature increased (Fig. 11(c)). However, drastic changes occurred in the 200-300 ℃ range. This phenomenon is closely related to the thermal activation process of interface traps.

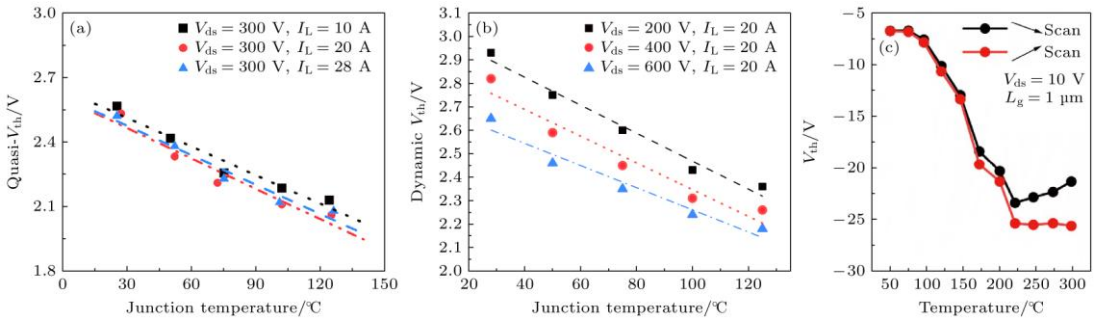


Fig. 11 (a) Variation of V_{Th} in SiC MOSFET with junction temperature under different load currents[54]; (b) temperature dependence of dynamic V_{Th} in SiC MOSFET under different V_{Th}[55]; (c) relationship between V_{Th} and junction temperature in Ga_2O_3 MOSFET[33].

2.5 Gate Leakage Current (I_{GLeak})

GaN HEMT devices incorporate various gate structures, as described in references [56-58]. For devices with a p-GaN structure (a Schottky junction without an additional insulating layer) [59], significant temperature dependence of I_{GLeak} is observed. The gate region of the tested device can be modeled as the p-GaN/AlGaN/GaN stack shown in Figure 12(a). Its electrical behavior is equivalent to two back-to-back diodes: a Schottky rectifier formed by the metal/p-GaN junction and a PiN rectifier constituted by the p-GaN/AlGaN/GaN structure [60]. Previous studies indicate that I_{GLeak} in Schottky metal/p-GaN contacts arises from the combined effects of multiple physical mechanisms. These primarily include two-dimensional variable-range hopping, thermionic field emission, and Poole-Frenkel emission [61,62]. The dominance of a specific mechanism depends on the gate bias and temperature

conditions.

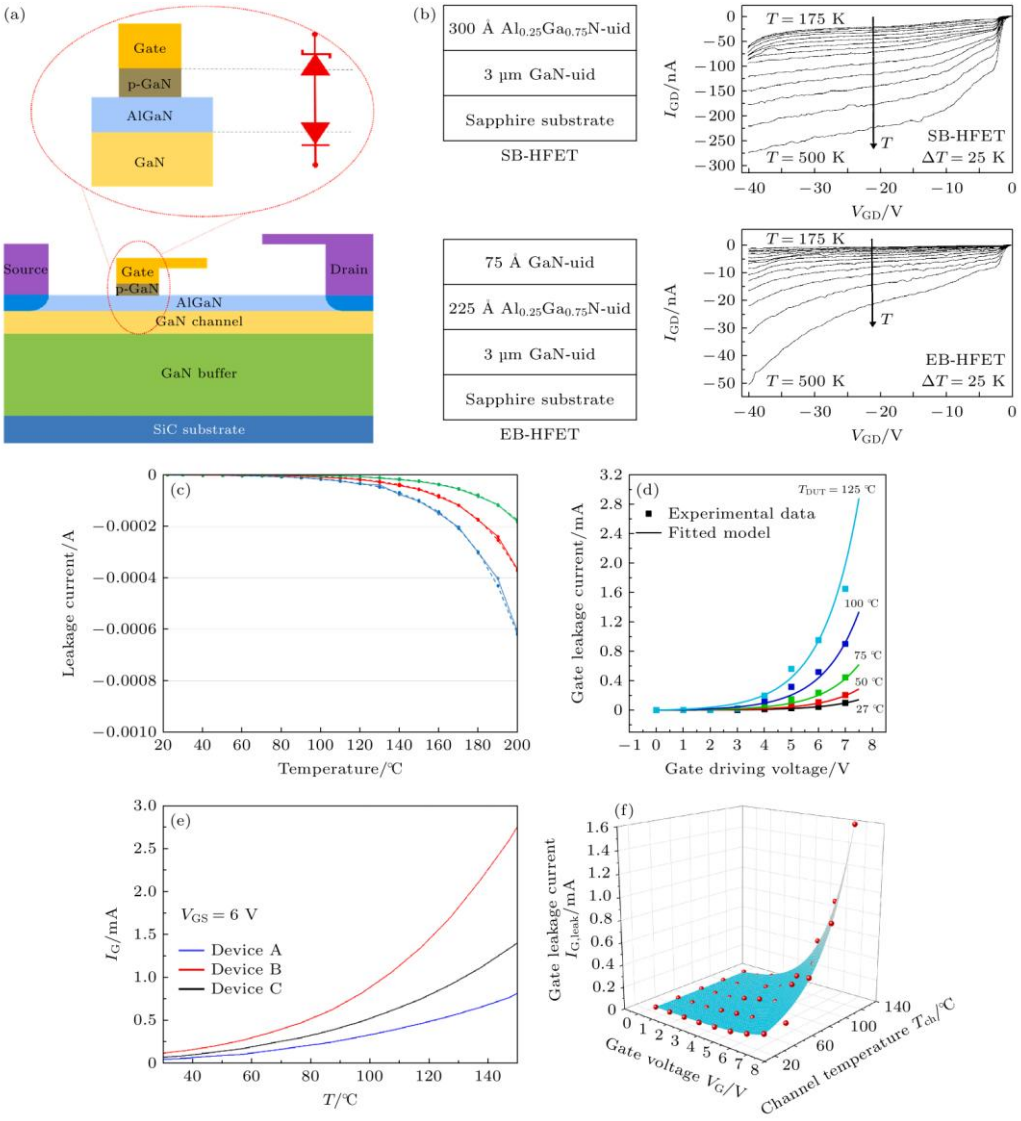


Fig. 12 (a) Cross-sectional schematic of a p-GaN HEMT, including a magnified view of the gate structure[60]; (b) temperature dependence of I_{GLeak} in SB-HFET and EB-HFET[63]; (c) the measured (solid line) and simulated (dashed line) I_{GLeak} of EPC2022 under conditions of V_{GS} = -4 V (blue), -3 V (red), and -2 V (green)[64]; (d) comparison of experimental and simulated I_{GLeak} at different temperatures[65]; (e) temperature calibration curves for three p-GaN devices[66]; (f) comparison of experimental and modeled I_{GLeak} under different channel temperatures and gate voltages[60].

Building on this foundation, researchers have systematically elucidated the temperature characteristics of I_{GLeak} from various perspectives. In early studies, Miller et al.[63] investigated the broader class of AlGaN/GaN heterojunctions. By comparing standard barrier (SB-HFET) and polarization-enhanced barrier (EB-HFET) structures, they established the temperature dependence of I_{GLeak} within the 175-500 K range (Fig. 12(b)). The study revealed that the leakage current in EB-HFETs could be more than an order of magnitude lower than that in SB-HFETs. This finding demonstrates that

"barrier engineering" is an effective strategy for regulating both the absolute magnitude of I_{GLeak} and its temperature sensitivity. With the widespread adoption of commercial GaN devices, the temperature characteristics of I_{GLeak} have undergone further quantitative validation. Roschatt et al.[64] observed two commercial GaN FETs, EPC2001 C and EPC2022. They noted that under gate voltages of 4-6 V, I_{GLeak} exhibited a clear exponential increase with rising temperature. The quantified sensitivity was approximately a 30% increase per 10 ℃ rise in temperature. Notably, experiments under negative gate bias conditions showed that the current increased by approximately 50% for every 10 ℃ rise in temperature (Fig. 12(c)). This observation provides an optimized direction for high-precision temperature monitoring.

In recent years, as p-GaN HEMTs have become a research focus, Borghese et al.[65] developed an online channel temperature monitoring method for p-GaN HEMTs based on I_{GLeak} detection. They first used TCAD simulations to reveal the high sensitivity of I_{GLeak} to temperature. Subsequently, they performed static characteristic calibration within the V_{GS} = 0-7 V range and the 25-150 ℃ temperature interval. This process established a relationship model between I_{GLeak} and p-GaN HEMT temperature, as shown in Fig. 12(d). The results indicated a nonlinear dependence between I_{GLeak} and device temperature. However, practical implementation of this method must account for device-to-device variations. The study by Franke et al.[66] confirmed this point. They measured three p-GaN devices under V_{GS} = 6 V conditions. While all devices confirmed the significant nonlinear characteristics between I_{GLeak} and temperature, the specific calibration curves showed distinct differences (Fig. 12(e)). Therefore, individual calibration for each device is essential to achieve precise temperature measurement. Synthesizing recent studies, Yin et al.[60] systematically analyzed the nonlinear dependence of I_{GLeak} on temperature for p-GaN HEMTs. They combined two-dimensional electro-thermal TCAD simulations with experimental validation. Their work explicitly identified the exponential growth characteristic of I_{GLeak} with increasing temperature (Fig. 12(f)). This study reaffirms the strong correlation of I_{GLeak} as an effective indicator for temperature monitoring.

2.6 Gate Resistance Thermometry

Gate resistance thermometry (GRT) is an electrical characterization technique. It determines the average temperature of the gate region in GaN HEMTs by measuring the resistance change of the gate metal during heating. Unlike methods that extract the average source-drain temperature from output characteristics or the average source-gate temperature from transfer characteristics, GRT reflects the temperature distribution within the gate-covered area. Since the highest device temperature typically occurs near the gate-covered region, this method is considered one of the most effective electrical approaches for evaluating the peak temperature of GaN HEMTs.

In early research, GRT was primarily used to measure the steady-state temperature of gate metals in multi-finger GaN HEMTs[67]. This measurement relies on the four-probe method, employing independent electrodes to record voltage and current separately. The measurement system is illustrated in Fig. 13(a). The key to GRT device layout design lies in introducing additional metal leads at the gate terminals. This forms a two-terminal gate test structure, enabling temperature measurement without powering down the device. Pavlidis et al.[68] conducted a comparative study on the thermal characteristics of GaN devices using GRT and Raman thermometry. They achieved the first experimental comparison of these two methods in multi-finger devices. As shown in Fig. 13(b), the gate channel temperature obtained by GRT aligns closely with Raman thermometry results under low power density and conventional bias conditions. However, under high power density conditions, Raman thermometry yields higher values than GRT measurements. This discrepancy arises mainly because local high-temperature peaks exist in the central region of the device, whereas GRT reflects the surface average temperature along the gate width direction.

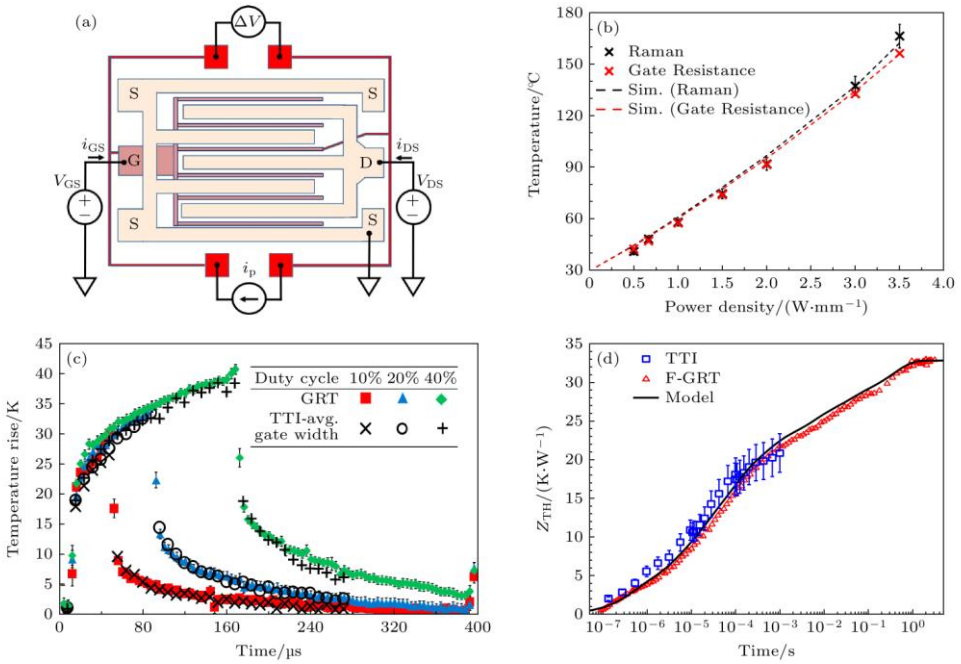


Fig. 13 (a) Device layout and GRT measurement setup[68]; (b) temperature measurement results from Raman spectroscopy and GRT, compared with finite element simulation[68]; (c) transient temperature rise of GaN HEMT at different duty cycles, measured by TTI and GRT[69]; (d) comparison of thermal impedance results from gate resistance frequency domain method, transient thermal model, and TTI measurement[70].

Beyond steady-state thermal characterization, GRT holds the potential for real-time monitoring of transient channel temperatures. Current studies have explored the transient thermal characteristics of GaN HEMTs in both the time and frequency domains. In most time-domain GRT measurements, a pulsed *I-V* system synchronized

with an oscilloscope typically biases the device while monitoring the voltage drop across the gate metal. Figure 13(c) presents the transient temperature variations of GaN HEMTs under different duty cycles as monitored by time-domain GRT. These results align closely with measurements obtained using thermoreflectance techniques[69]. Furthermore, another approach for assessing the transient temperature of GaN HEMTs involves monitoring gate thermal resistance in the frequency domain. Cutivet et al.[70] first reported frequency-domain GRT experiments, applying a sensing current to the gate and a frequency-dependent AC bias to the drain. A lock-in amplifier serves as a key component in this system, enhancing the signal-to-noise ratio of GRT measurements under fixed-frequency bias. Figure 13(d) compares the thermal impedance results from frequency-domain GRT, TTI, and thermal network models. The three datasets demonstrate high consistency across time scales.

2.7 Diode Junction Voltage Method

The temperature-sensitive property of the diode junction voltage, commonly known as the "diode junction voltage method," represents one of the most core and widely applied techniques for electrical temperature measurement in wide-bandgap semiconductor devices. Its fundamental principle involves applying a constant current bias to a semiconductor PN junction or Schottky junction and inferring temperature from the relationship between junction voltage and temperature. This principle underpins many commercial high-precision junction temperature measurement instruments, such as the Simcenter Micred T3STER from Siemens and the Phase 12 thermal analyzer from Analysis Tech.

For wide-bandgap semiconductor power devices, this method requires adaptation based on their specific device physics and structural features. For SiC MOSFETs, the inherent parasitic body diode can serve as a built-in temperature sensor. For instance, Gonzalez and Alatise[71] systematically investigated the junction temperature measurement characteristics using the forward voltage (V_{SD}) of the SiC MOSFET body diode as a temperature-sensitive parameter. They also examined the influence mechanism of bias temperature instability (BTI). They first calibrated the temperature characteristics of V_{SD} over a range of 25—150 ℃ using a temperature-controlled stage (Figure 14(a)). They found that when the gate voltage V_{GS} = 0 V, the measured V_{SD} value (approximately 1.5 V) was significantly lower than the true body diode voltage drop due to partial channel conduction caused by the body effect. However, when $V_{GS} = -10$ V completely turned off the channel, V_{SD} rose to approximately 3 V, exhibiting typical P-N junction characteristics. Zhu et al.[72] innovatively employed a dual-current measurement method. By compensating for the difference in intercepts at absolute zero between the two diode junction voltage-temperature curves, they effectively eliminated measurement errors caused by the temperature dependence of the ideality factor in

traditional methods. Figure 14(b) shows the test results for SiC MOSFETs. Within the temperature range of −50—170 ℃, the temperature measurement error of this method remains below 2.2%.

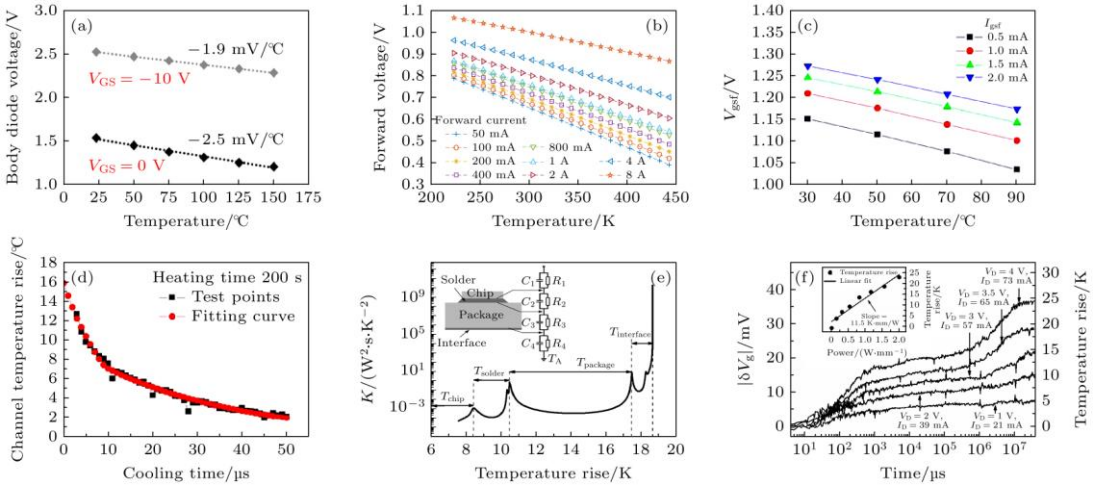


Fig. 14 (a) Forward voltage of the SiC MOSFET body diode as a function of temperature for different gate voltages[71]; (b) relationship between the junction voltage of the SiC MOSFET body diode and temperature under different forward currents[72]; (c) V_{GSf} versus temperature for GaN HEMT[77]; (d) cooling curve of channel temperature[77]; (e) temperature rise extracted for each material layer using the structure function method. Inset: Foster RC network model[78]; (f) transient temperature rise curves of the device under different electrical bias conditions, with the inset showing the relationship between temperature rise and power density[78].

Unlike SiC MOSFETs, GaN HEMTs lack a body diode. However, the Schottky junction naturally formed between the gate metal and the AlGaN barrier layer (or the corresponding junction in p-GaN gate structures) can be effectively utilized. By applying a small forward bias current to the gate (with the Schottky junction voltage denoted as V_{GSf}) and measuring the forward voltage drop of this junction, the junction temperature can be inferred[73,74]. The physical principle is identical to the diode junction voltage method described above. The primary challenge lies in the fact that GaN HEMTs typically operate with negative or zero gate bias to control channel conduction, whereas temperature measurement requires forward bias. Consequently, implementation requires completely turning off the device power (V_{DS} and V_{GS}) within an extremely short time window, followed by rapid injection of the measurement current and acquisition of the V_{GSf} signal. This imposes stringent requirements on the timing precision of the measurement and control system[75,76]. To address this challenge, Feng et al.[77] employed a high-speed (1 MHz) and high-resolution sampling board as the core component. Controlled by a computer-driven switching circuit, this setup completes the conversion within 3 μs. The GaN HEMT was heated under different constant currents (0.5-2.0 mA). As shown in Fig. 14(c), V_{GSf} exhibits a good linear decreasing trend with temperature (from room temperature to 250 ℃), with a

temperature coefficient of −1.65 to −1.95 mV/K, establishing a reliable voltage-temperature correspondence. To capture the temperature at the instant of power-off, the cooling curve of V_{GSf} was acquired and extrapolated via exponential regression. As illustrated in Fig. 14(d), this approach accurately obtained the channel temperature at the moment of power shutdown. Zhang et al.[78] also leveraged the temperature-sensitive characteristics of V_{GSf} to systematically investigate the transient temperature rise and cross-sectional temperature distribution of GaN HEMTs under various power conditions. As indicated in Fig. 14(e), the transient temperature rise curve displays three steps in logarithmic coordinates, corresponding to the chip layer, solder layer, and package layer, respectively. The temperature rise contribution of each material layer was further extracted using the structure function method, as shown in Fig. 14(f). For instance, at V_{DS} = 3.5 V and I_{DS} = 65 mA, the temperature rises for the chip, solder, and package layers were 8.4 ℃, 2 ℃, and 7 ℃, respectively.

2.8 Turn-on Delay Time

The turn-on delay time refers to the critical time interval from the change in the gate drive signal to the onset of I_{DS} response, reflecting the device's response speed during switching. Based on this, Pan et al.[79] developed a method for measuring GaN HEMT junction temperature using turn-on delay time with sinusoidal signals. They systematically studied the effects of temperature (30-180 ℃) and bias voltage on electron transport characteristics in the saturation region. As shown in Fig. 15(a), a 50 mV sinusoidal signal was superimposed on V_{GS}. The time interval between the input voltage peak and the I_{DS} response peak was precisely captured as the turn-on delay time, effectively avoiding errors caused by oscillations in pulse signal measurements. As depicted in Fig. 15(b), at a fixed V_{DS}, the delay time exhibits a non-monotonic trend with increasing temperature: the delay time increases in the low-temperature range, primarily due to the decrease in carrier saturation drift velocity with rising temperature; conversely, the delay time shortens in the high-temperature range, which is associated with the weakening of charge trapping effects as temperature increases.

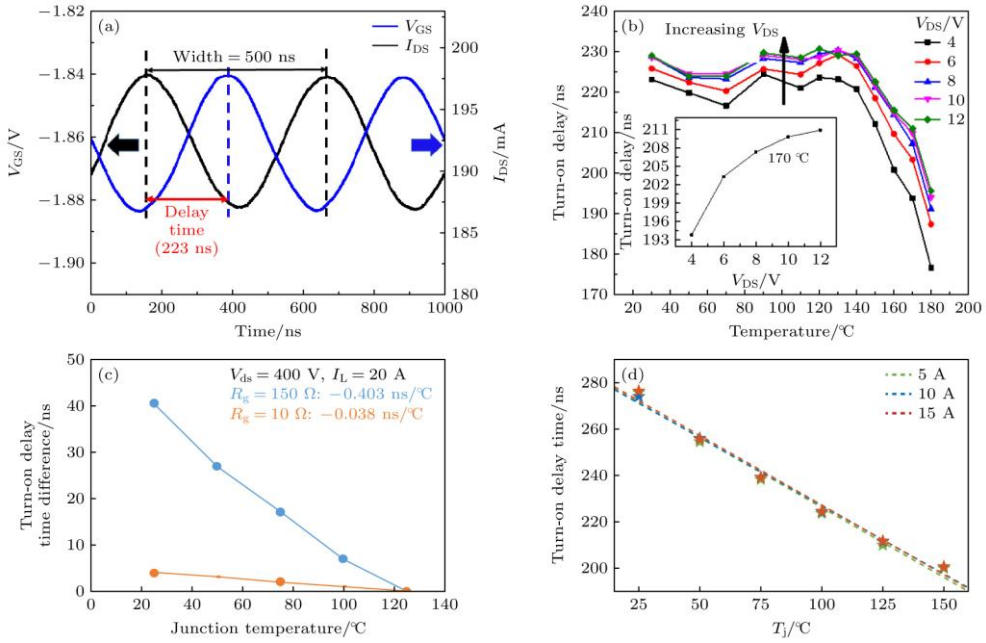


Fig. 15 (a) Turn-on delay between the V_{GS} peak and the corresponding I_{DS} peak[79]; (b) relationship between the turn-on delay time and temperature for a GaN HEMT, the inset shows the curve of turn-on delay versus V_{DS} at 170 ℃[79]; (c) temperature dependence of turn-on delay time under different gate resistances[80]; (d) relationship between turn-on delay time and junction temperature under different load currents[81].

Qiao et al.[80] utilized turn-on delay time as a temperature-sensitive parameter to measure the junction temperature of SiC MOSFETs and developed an intelligent gate driver integrating this function. By dynamically switching the gate resistance (increasing from 10 Ω for normal operation to 150 Ω), they improved the temperature sensitivity from -0.038 ns/℃ to -0.403 ns/℃, achieving an enhancement of more than tenfold (Fig. 15(c)). Yang et al.[81] employed the same circuit and further discovered that the turn-on delay time of SiC MOSFETs is insensitive to load current, as shown in Fig. 15(d). This finding demonstrates that the technique is particularly suitable for junction temperature testing in parallel device configurations.

In summary, the advantage of electrical methods lies in their ease of implementing online, real-time monitoring without requiring structural modifications to the device for in-situ measurement[82]. However, different temperature-sensitive parameters vary significantly in practicality and must be selected according to the specific device type. As shown in Table 1, implementation difficulty refers to the complexity of incorporating the parameter into a circuit for temperature measurement. This primarily depends on whether the required peripheral circuitry is complex, easy to integrate, and whether precise and tedious calibration is necessary. Self-heating impact refers to the extent to which internal heating generated by the device during the measurement process affects the final temperature measurement accuracy. The more significant the

self-heating effect, the poorer the real-time performance and accuracy of the temperature measurement. Although some temperature-sensitive parameters offer advantages such as excellent linearity, high sensitivity, and relative ease of implementation, electrical methods generally characterize the spatially averaged temperature of a specific region (such as the channel or junction area). This average value often severely underestimates the actual maximum junction temperature of the device. This is particularly true for power devices with pronounced self-heating effects, where heat flow distribution is highly non-uniform, and internal temperature gradients within a single device can reach tens or even hundreds of degrees Celsius[83]. Furthermore, the accuracy of this method heavily depends on the calibration precision of the temperature-sensitive parameter and is susceptible to interference from factors such as device aging and self-heating effects[84], necessitating effective separation of these influences in practical applications. For devices such as GaN HEMTs, trap effects and current collapse effects further perturb the temperature response characteristics of temperature-sensitive parameters, thereby reducing measurement accuracy[85,86]. In SiC MOSFETs, gate oxide interface states and the nonlinear temperature dependence of channel mobility may also introduce similar errors. For Ga_2O_3 devices, especially Schottky barrier diodes (SBDs), their extremely low thermal conductivity and defect-related electrical instability pose greater challenges to the stable extraction of temperature-sensitive parameters under high-temperature and high-voltage conditions.

Table 1. Comprehensive comparison of temperature sensitive parameters used in electrical methods.

Temperature sensitive parameter	Linearity	Sensitivity	Temperature coefficient	Self-heating effect	Realization difficulty	Applicable device
On-resistance	Difference	Medium	Positive	Medium	Yi	GaN, SiC, Ga_2O_3 device
Saturation leakage current	Excellent	High	Negative	High	Yi	GaN, Ga_2O_3 device
	Excellent	High	Positive	High	Yi	SiC device
Threshold voltage	Excellent	High	Change	Low	Difficult	GaN device
	Excellent	High	Negative	Low	Difficult	SiC device
	Difference	High	Change	Low	Difficult	Ga_2O_3 device
Grid leakage current	Difference	Medium	Positive	Medium	Difficult	GaN device
Grid resistance	Excellent	High	Positive	Low	Difficult	GaN device
Diode junction voltage	Excellent	High	Negative	Low	Yi	GaN, SiC device
Switching delay time	Difference	Medium	Change	Low	Difficult	GaN device
	Excellent	Medium	Negative	Low	Difficult	SiC device

Therefore, although electrical methods offer irreplaceable value for real-time monitoring, their effectiveness is comprehensively constrained by parameter selection, device type, and operating environment, as systematically compared in Table 1. In practical applications, one must carefully balance the linearity, sensitivity, implementation difficulty, and compatibility of different temperature-sensitive parameters with specific devices (such as GaN, SiC, or Ga_2O_3). Furthermore, calibration and compensation strategies should be employed to overcome their inherent limitations.

3 Physical Contact Methods

Physical contact methods constitute a class of techniques that acquire temperature information by detecting changes in the physical properties of measurement probes, sensors, or thermosensitive materials. These materials undergo direct or indirect heat conduction with the surface or interior of the device under test. Primary techniques include scanning thermal microscopy, thermocouples/thermistors, micro-integrated temperature sensors, and nematic liquid crystal imaging. Consequently, this section reviews research progress on measuring the junction temperature of wide-bandgap semiconductor devices using these technologies, covering testing principles, results, and accuracy analysis.

3.1 Scanning Thermal Microscopy (SThM)

SThM is a technique derived from atomic force microscopy (AFM) that provides extremely high spatial resolution (nanometer scale) in thermal measurements[87,88]. Various solutions exist for integrating thermal probes into AFM systems. Kuball et al.[89] directly integrated nanoscale thin-film thermocouples at the tip of the AFM probe (see inset in Figure 16(b)). Theoretically, SThM offers nanoscale spatial resolution, which is primarily limited by the radius of the scanning probe tip. Regarding measurement accuracy, the finite thermal resistance between the SThM probe and the device surface must be carefully considered. This thermal resistance is influenced by variations in surface roughness across different regions of the GaN HEMT (Figure 16(a)), although the thermal conductivity of the surface material also plays a significant role. After appropriate calibration, temperature distribution maps can be generated, as shown in Figure 16(b). Gucmann et al.[90] also fabricated nanoscale metal thin-film thermocouples on AFM probes. They systematically evaluated scanning SThM for nanoscale temperature measurement of GaN HEMTs in both contact and tapping modes. As shown in Figure 16(c), measurements in both modes agreed well with simulation results (deviation ±3 ℃), demonstrating the potential of SThM for precise nanoscale temperature measurement. However, the study also noted a 15%-44% deviation between measured temperatures and simulation results in two-dimensional temperature mapping. This discrepancy mainly arose because the SThM probe did not reach thermal steady state within the limited pixel dwell time (approximately 4.9-20 ms in contact mode and 170-310 μs in tapping mode). To enhance temperature measurement sensitivity, Aubry et al.[91] deposited a palladium metal thin film on the AFM probe tip, creating a resistive scanning thermal probe (Figure 16(d)). Using this probe, they performed nanoscale temperature mapping of GaN HEMTs under different DC biases. As shown in Figure 16(e), at a power density of 8.8 W/mm (V_{GS} = -2 V, V_{DS} = 18.2 V), the highest measured temperature (154 ℃) was located at the drain-side

edge of the gate. The temperature gradually decreased along the gate toward the drain, dropping by approximately 16 ℃ near the drain contact region, thereby clearly revealing the lateral thermal gradient of the device.

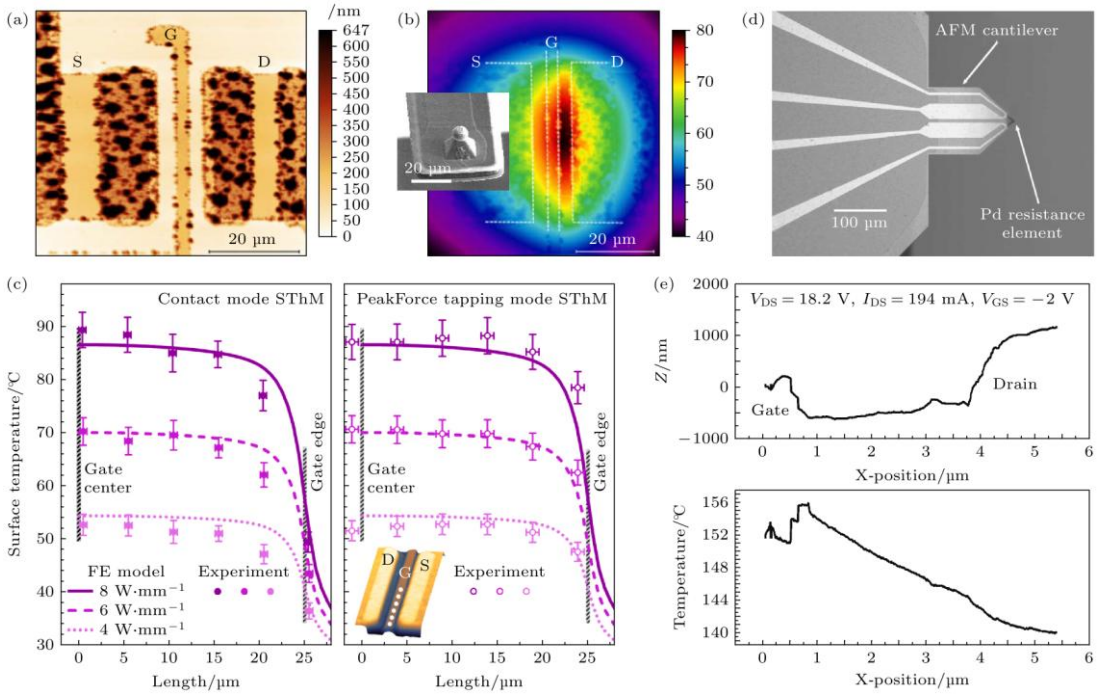


Fig. 16 (a) Surface topography of the GaN HEMT measured by SThM[89]; (b) temperature distribution measured by SThM, with the inset showing the AFM probe integrated with a thermocouple[89]; (c) temperature measurements of the GaN HEMT in contact mode and tapping mode, compared with finite element simulation results[90]; (d) AFM probe integrated with a resistive temperature sensor[91]; (e) cross-sectional topography and thermal imaging of the GaN HEMT[91].

3.2 On-chip integrated thermocouples and resistance temperature detectors

Thermocouples (TCs) operate based on the thermoelectric effect (Seebeck effect). When two distinct conductors form a closed loop with different temperatures at their junctions, a thermal electromotive force is generated. The magnitude of this electromotive force depends on the temperature difference between the hot and cold junctions, typically exhibiting a nonlinear relationship. By precisely measuring this electromotive force and combining it with the known cold junction temperature, the measured temperature at the hot junction can be determined. Bhatti et al.[92] achieved monolithic integration of micro-film thermocouples on GaN HEMTs. This study employed platinum-chromium junctions as temperature sensing units. The thermocouples, with micrometer-scale widths, were fabricated directly in the channel region between the gate and drain of the device, as shown in Figure 17(a). In measurements of GaN HEMTs (with a gate width of 200 μm), the integrated micro-film thermocouples monitored channel temperature variations under different output power

densities. These measurements showed high consistency with model predictions (Figure 17(b)). Bhatti et al.[93] integrated micro-film thermocouples (micro-TFTCs) on multi-finger Ga_2O_3 MOSFETs. The schematic of the integration structure is shown in Figure 17(c). They verified that the sensitivity of the micro-TFTCs reached (19.23±0.41) μV/℃.

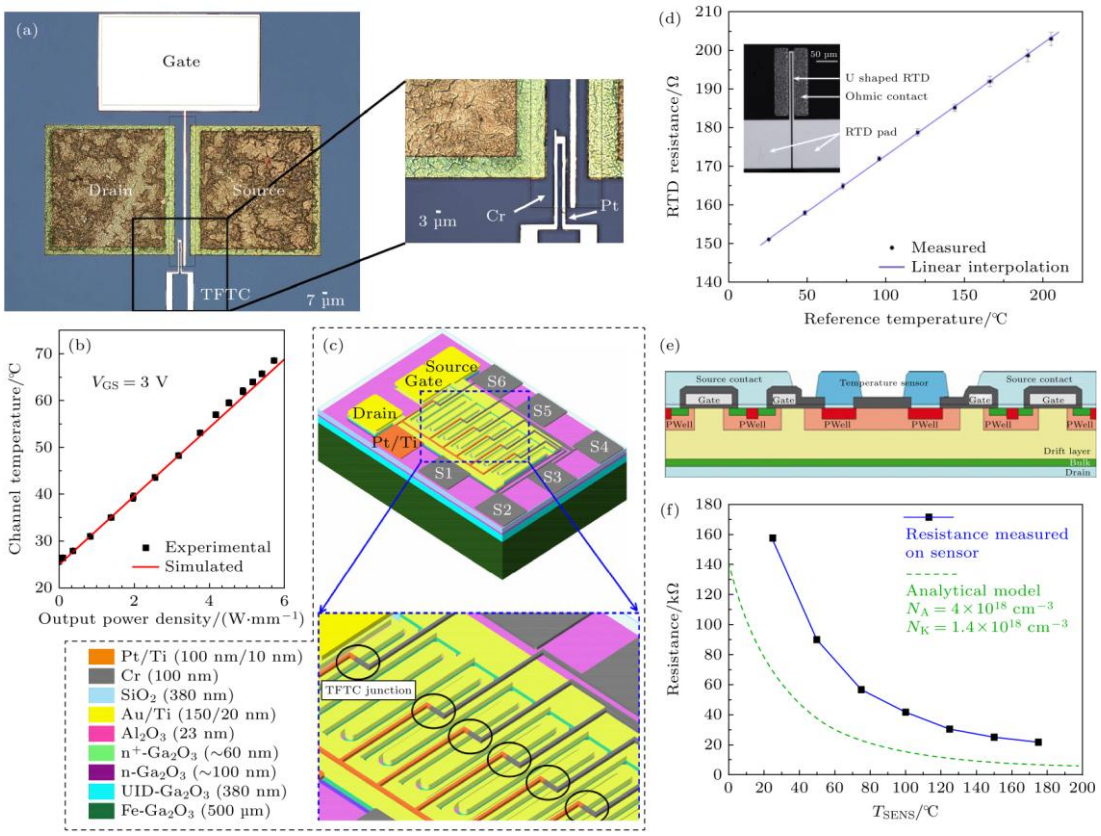


Fig. 17 (a) Top view of the GaN HEMT device; the enlarged diagram indicates the placement of the micro thin-film thermocouple[92]; (b) relationship curve between channel temperature and power density[92]; (c) 3D model of multi-finger Ga_2O_3 MOSFET integrated with TFTCs[93]; (d) resistance-temperature (*R-T*) calibration curve; the inset shows the position of the integrated RTD[94]; (e) schematic diagram of the integration of resistive temperature sensors in the active region of SiC MOSFETs[95]; (f) temperature dependence of resistive temperature sensors[95].

Thermal resistance (TR) sensing relies on the temperature-dependent resistance of metallic conductors or semiconductors. As temperature rises, resistance increases, allowing temperature calculation through resistance measurement. Arenas et al.[94] investigated the feasibility of integrating platinum micro-resistance temperature detectors (RTDs) into gateless GaN HEMT devices for direct channel temperature measurement. This study integrated a U-shaped platinum micro-resistor structure (328 μm × 3 μm) between the source and drain electrodes (see inset in Figure 17(d)). A four-wire floating configuration ensured electrical independence between the sensor and the device. As shown in Figure 17(d), the RTD exhibited a strong linear response

over the range of 0-206 ℃, with a temperature coefficient α = 2.0227×10^{-3} ℃$^{-1}$. Comparison of three-dimensional finite element thermal simulations with experimental data revealed that the average temperature measured by the micro-RTD ($\overline{T}_{\mathrm{RTD}}$) closely matched the simulated average channel temperature ($\overline{T}_{\mathrm{CHS}}$) within the 0.1-1 W power range. The maximum deviation was only 4.4 ℃. Berthou et al.[95] reported the first monolithic integration of resistive temperature sensors in SiC MOSFETs. As illustrated in Figure 17(e), the sensor forms ohmic contacts with the p-well layer via two independent electrodes. It shares the epitaxial structure with the power MOSFET while maintaining electrical isolation. Calibration results indicated that the sensor resistance decreased monotonically over the 25-175 ℃ range. Although measured resistance values exceeded theoretical predictions due to contact quality issues (Figure 17(f)), the temperature sensitivity remained sufficient to achieve a measurement accuracy of approximately 10 ℃.

3.3 Nonlinear Element Temperature Sensors

In GaN HEMT junction temperature measurement technology, nonlinear element temperature sensors fall into two main categories: discrete devices and monolithically integrated devices. The core distinction lies in their device structures and integration methods.

Discrete devices refer to independently fabricated sensing units with single functions. They typically connect to power devices via peripheral circuits. Typical examples include Schottky barrier diodes (SBDs)[96-101], P-N junction diodes[102], and mixed-anode diodes[103]. The threshold voltage (V_{Th}) of an SBD is approximately one-third to one-half that of a P-N junction diode. This indicates that SBDs offer greater advantages for low-power in-situ monitoring. Based on this, Pu et al.[96] investigated two types of recessed-anode AlGaN/GaN SBDs, as shown in Figure 18(a). As illustrated in Figure 18(b), at current levels of 1×10^{-5}, 1×10^{-6}, and 1×10^{-7} A, the temperature sensitivities of the conventional anode SBD (CA-SBD) were approximately 1.26, 1.44, and 1.61 mV/K, respectively. In contrast, the sensitivities of the recessed anode SBD (RA-SBD) were approximately 0.78, 0.95, and 1.05 mV/K, respectively. To further enhance temperature sensitivity, Sun et al.[97] proposed a GaN/AlGaN/GaN SBD temperature sensor based on a thin AlGaN barrier layer and a recessed anode, as shown in Figure 18(c). By reducing the two-dimensional electron gas density, this design suppresses the proportion of tunneling current. This makes the current transport mechanism closer to thermionic emission dominance. At an extremely low current of 1×10^{-7} A, the device achieved a high sensitivity of 1.39 mV/K and a linearity of 0.995. Yan et al.[98] proposed a PCT-SBD structure featuring a partial p-GaN cap layer and a semi-circular T-shaped anode, as shown in Figures 18(d) and (e). By adjusting the position of the subthreshold region, the sensitivity reached

2.54 mV/K at a current density of 2.04 A/cm^2. In 2025, Sun et al.[99] reported a novel discrete GaN/AlGaN/GaN SBD thermal sensor based on a thick GaN cap layer, as shown in Figures 18(f) and (g). This device achieved a sensitivity as high as 13.3 mV/K and a linearity of 0.992 at a fixed current of 10^{-5} A over the temperature range of 298-573 K.

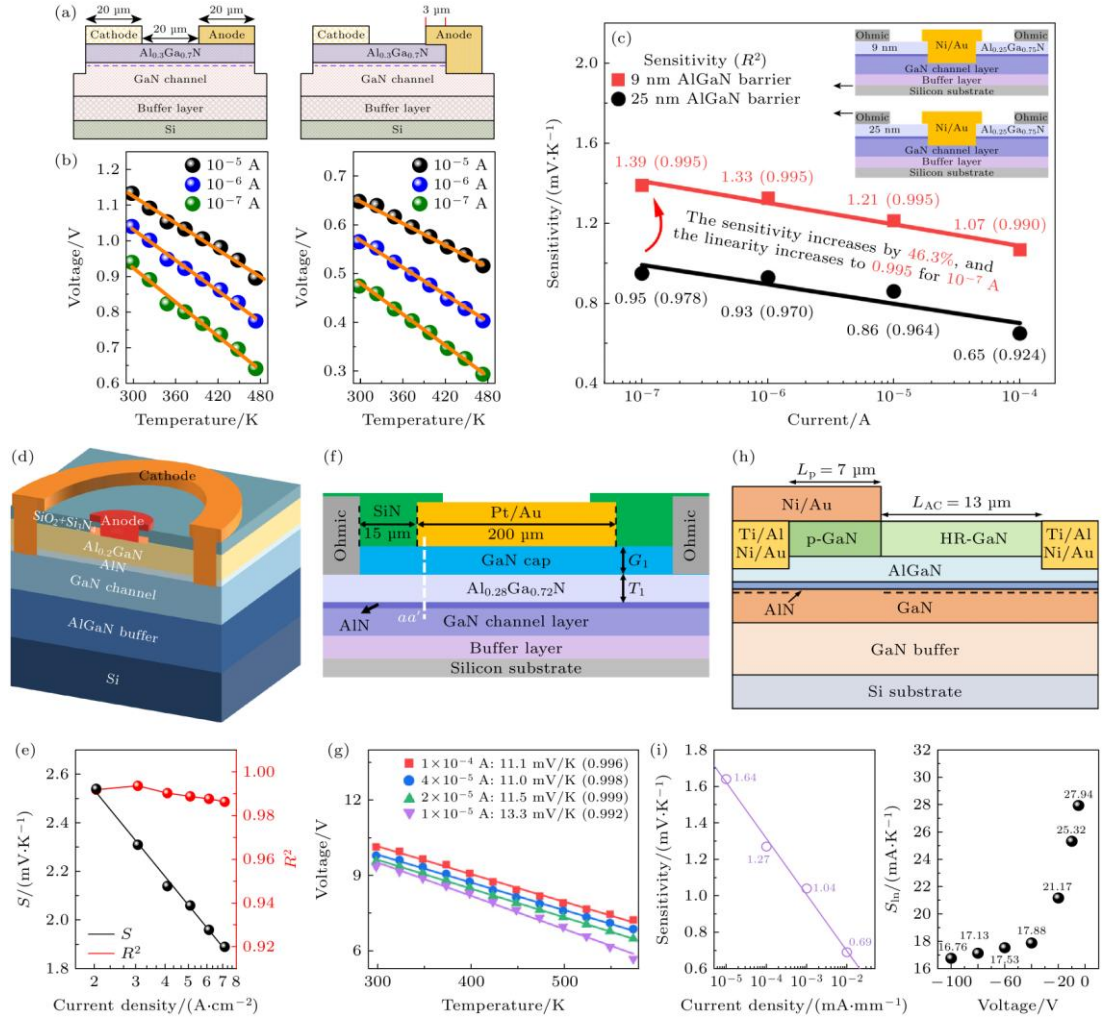


Fig. 18 (a) Cross-sectional views of the CA-SBD (left) and RA-SBD (right)[96]; (b) forward voltage versus temperature at various current levels for the CA-SBD and RA-SBD, shown in the left and right panels, respectively[96]; (c) relationship between sensitivity and current, with an illustration showing the cross-sectional schematic of an AlGaN/GaN SBD thermal sensor[97]; (d) structure of the PCT-SBD[98]; (e) temperature sensitivity (*S*) and goodness of fit (R^2) versus current density[98]; (f) schematic cross-sectional view of the thick-cap AlGaN/GaN SBD thermal sensor[99]; (g) experimental relationships of voltage versus temperature[99]; (h) schematic device structures of the HAD[103]; (i) sensitivity analysis under forward and reverse bias[103].

The hybrid anode diode (HAD) combines the advantages of p-GaN gates and Schottky contacts to form a temperature sensor with a dual-sensing mechanism. Wei et al.[103] reported a temperature sensor based on lateral p-GaN/AlGaN/GaN HADs that exhibits

dual current and voltage sensitivity (Fig. 18(h)). As shown in Fig. 18(i), under forward bias, the voltage sensitivity reaches 1.64 mV/K at a specific anode current density. Under reverse bias, the leakage current also demonstrates temperature dependence, with a sensitivity as high as 27.94 mA/K (at −5 V), offering an alternative approach for temperature sensing.

Monolithically integrated devices refer to the integration of temperature sensing units and power devices on the same chip, achieving direct interconnection through shared epitaxial layers and processes. Such devices offer advantages including fast response, low parasitic parameters, and high compatibility, making them more suitable for high-density power integrated circuits. For instance, Chang et al.[104] connected a two-dimensional electron gas (2DEG) resistor in series with a PiN diode using a p-GaN/AlGaN/GaN heterojunction (Fig. 19(a)). By leveraging their opposite temperature characteristics (resistance increases with temperature, while the diode turn-on voltage decreases), they achieved a sensitivity of 19.7 mV/℃ at a 10 V bias, as shown in Fig. 19(b). To further enhance integration and sensitivity, Li et al.[105] proposed a four-transistor (4T) monolithic integration scheme for temperature sensing. The integrated structure is shown in Fig. 19(c), comprising direct-coupled FET logic (DCFL) and resistor-transistor logic (RTL) inverters. Specifically, the RTL inverter using a 2DEG resistor as the load achieves a sensitivity of up to 31.28 mV/℃ in the range of 25—250 ℃, with a linearity of R^2 = 0.995 and an error of only ±2.74 ℃ (Fig. 19(d)).

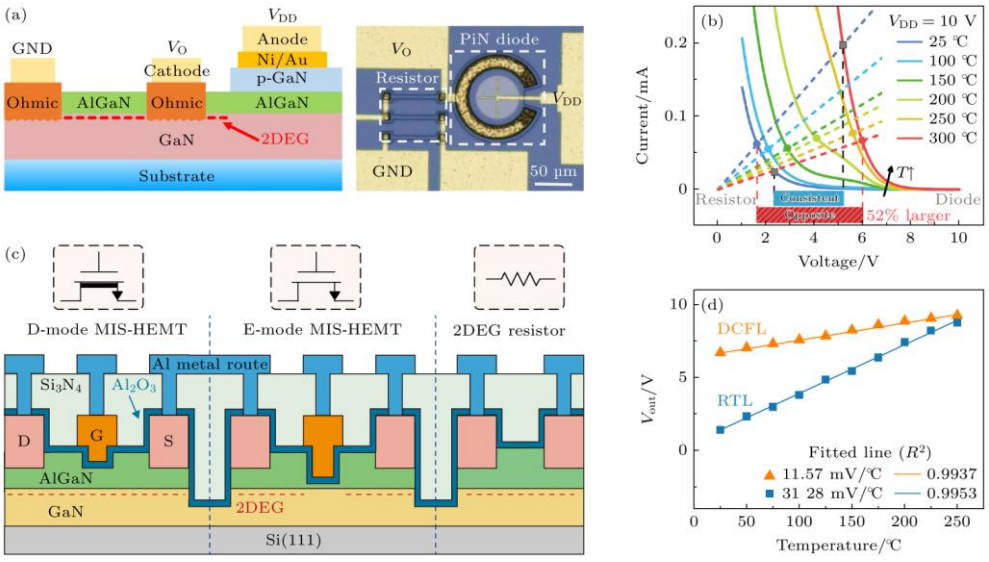


Fig. 19 (a) Structural schematic and photomicrograph of the integrated sensor in a GaN HEMT; (b) load curve comprising a series PiN diode and a two-dimensional electron gas resistor; (c) schematic cross-section of monolithically integrated D/E-mode GaN MIS-HEMTs and a two-dimensional electron gas resistor[105]; (d) relationship between the output performance of DCFL and RTL sensors and temperature[105].

3.4 Contact Optical Junction Temperature Measurement

Contact optical temperature measurement based on temperature-sensitive optical materials involves directly coating or placing photosensitive or fluorescent materials on the device surface. High-resolution temperature imaging is then achieved through optical observation, such as microscopy or fluorescence excitation.

Nematic liquid crystals are organic compounds existing between the solid state and the isotropic liquid state, possessing unique optical properties. Their molecules typically exhibit a helical structure, with a pitch on the same order of magnitude as the wavelength of visible light. This pitch changes with temperature, thereby affecting the wavelength-selective scattering of incident light. Consequently, the apparent color of the observed area changes continuously with temperature. By adjusting the chemical composition, the color-display temperature range of liquid crystals can be customized. Currently, the operating temperature range of commercial liquid crystal materials is −30—120 ℃, and the temperature response bandwidth can be adjusted between 0.5 and 30 ℃[106–108]. Commercial nematic liquid crystal materials typically achieve a spatial resolution of approximately 1 μm and a temperature resolution of 0.1 ℃[109].

Based on these temperature-sensitive chromogenic properties, liquid crystal imaging technology has been widely reported for junction temperature measurement in GaN HEMTs. Park et al.[108] systematically investigated the thermal characteristics of double-finger-gate GaN HEMTs using nematic liquid crystal thermography. The experiment employed nematic liquid crystal coatings with transition temperatures of 67 ℃ and 83 ℃. When the device surface temperature reached the liquid crystal phase transition point, distinct dark hot-spot regions were observed under a polarizing microscope. The experimental results showed that at a power dissipation of 0.29 W, the measured and simulated values were 67 ℃ (left panel of Figure 20(a)) and 66 ℃, respectively. At a power dissipation of 0.42 W, the measured hot-spot temperature was 83 ℃ (right panel of Figure 20(a)), which agreed well with the simulated hot-spot temperature of 85 ℃, verifying the accuracy of this method. The study also found that as power dissipation increased to 0.87 W, the hot-spot region expanded toward the drain and exhibited an irregular distribution (Figure 20(b)), reflecting the non-uniformity of channel current density. This method achieved a spatial resolution of 1 μm and a temperature accuracy of ±1 ℃. Hwang et al.[110] directly observed the evolution of surface hot spots in GaN HEMTs using nematic liquid crystal coatings. As shown in Figure 20(c), under drive conditions of 2.95 V/8.1 mA, a hot spot of approximately 80 μm first appeared in the cathode region. As power increased, the hot spot gradually expanded to 400 μm, covering the entire chip area (330 μm × 330 μm).

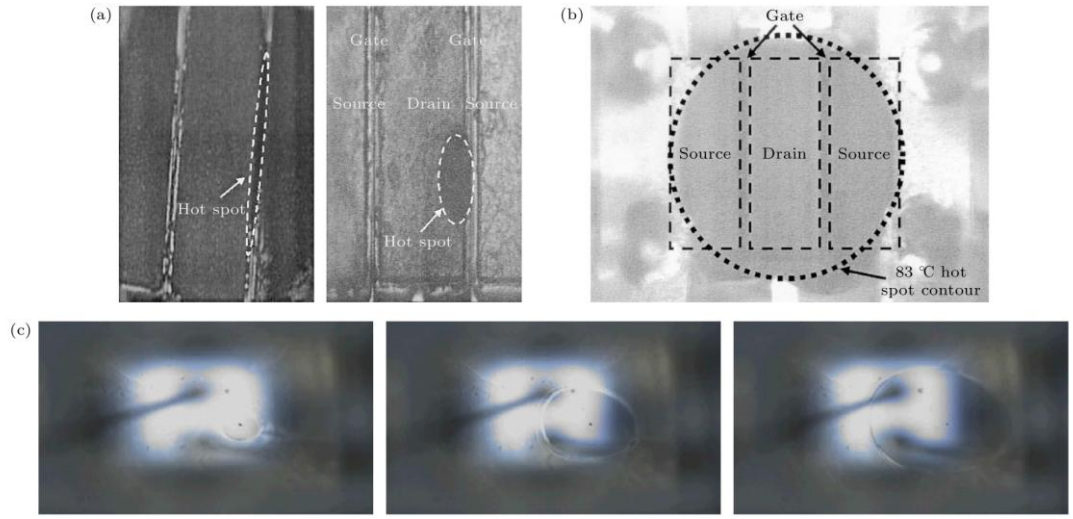


Fig. 20 (a) Liquid crystal imaging results of GaN HEMT[108]; (b) Liquid crystal imaging results of the GaN HEMT source, gate, and drain[108]; (c) Micrograph of the hotspot, showing gradual expansion over time[110].

Beyond nematic liquid crystal imaging, several novel contact-based optical temperature sensing techniques developed in recent years have demonstrated promising performance in micro- and nanoscale temperature measurement. In principle, these techniques can be extended to characterize the junction temperature of wide-bandgap semiconductor devices. Thermoluminescent phosphors[111,112] are a class of ceramic materials doped with rare-earth ions. Under ultraviolet excitation, they emit fluorescence, with intensity or lifetime varying with temperature. These materials offer a broad operating temperature range and excellent high-temperature resistance. Similar to liquid crystal imaging, they can be applied to device surfaces in the form of powders or slurries. Upconversion nanoparticles (UCNPs)[113,114] are typically doped with rare-earth ions such as Er^{3+}, Yb^{3+}, or Tm^{3+}. Under near-infrared excitation, they produce upconversion luminescence. The intensity ratio of emission from thermally coupled energy levels is highly sensitive to temperature, enabling self-calibrated temperature measurement. Furthermore, UCNPs offer low background noise and potential for microscale imaging.

In summary, physical contact methods such as scanning thermal microscopy, thermocouples, and thermal resistors offer advantages in spatial resolution and absolute temperature accuracy. However, these methods generally suffer from uncertainties introduced by probe-sample contact conditions. Minor variations in contact thermal resistance, tip pressure, and surface roughness can lead to significant measurement deviations. Specifically for scanning thermal microscopy, the thermal capacitance of the probe introduces additional thermal disturbances during transient measurements, thereby affecting the accurate characterization of the true junction temperature[115,116]. Moreover, for modern packaged wide-bandgap semiconductor devices with complex

multilayer structures (such as GaN HEMT active regions deeply buried under passivation layers and field plates), physical probes cannot directly access the heat source. Consequently, the measured signal represents the result of thermal crosstalk through multiple layers, severely limiting the accurate characterization of transient junction temperatures and true peak temperatures. Temperature sensing techniques based on active devices achieve fast response speeds and high integration by directly reading changes in electrical parameters, making them suitable for in situ junction temperature monitoring. However, their measurement accuracy and stability depend on device structure and bias conditions. Contact-based optical junction temperature measurement methods achieve high-spatial-resolution temperature imaging using temperature-sensitive materials. Future research should further explore their application in measuring the junction temperature of wide-bandgap semiconductor devices. Overall, each method has distinct advantages and limitations regarding spatial resolution, temporal response, integration difficulty, and engineering feasibility. Therefore, rational selection and synergistic application are required based on the structure and application scenarios of wide-bandgap semiconductor devices.

4 Optical Methods

As important non-contact approaches, optical methods offer unique advantages in spatial resolution, measurement speed, and applicability[117-122]. This section focuses on reviewing several mainstream optical measurement techniques, including infrared thermography, Raman imaging, and thermoreflectance. We systematically elucidate their working principles, technical characteristics, and scope of application. Furthermore, we analyze the advantages and limitations of these techniques when addressing the complex structures and high heat flux densities of wide-bandgap semiconductor devices.

4.1 Infrared Thermography

Infrared thermography is currently one of the primary techniques used in industry for temperature measurement of semiconductor devices and circuits[123-125]. This technique detects thermal radiation emitted from the surface of the object under test using corresponding detectors. According to the Stefan-Boltzmann law, thermal radiation intensity is proportional to the fourth power of the absolute surface temperature. Therefore, if the surface emissivity is known, the temperature can be determined by measuring the radiation intensity. However, because real device surfaces are not ideal blackbodies (emissivity < 1), emissivity calibration is required before temperature measurement[126,127]. The typical procedure involves mounting the device on a temperature-controlled stage. At this uniform temperature, the infrared camera captures a thermal image. Theoretically, the temperature at every pixel should be identical. Any

brightness difference between pixels is solely due to variations in material emissivity. The software calculates a normalization coefficient for each pixel so that the entire image displays a uniform temperature at the calibration temperature[128-131]. Additionally, considering that semiconductor device surfaces usually consist of different materials (such as the semiconductor bulk, passivation layers, and metal contact regions), their emissivities vary spatially. Therefore, calibration must be performed on a pixel-by-pixel basis. Surfaces with low emissivity or transparency require coverage with an opaque, high-emissivity "black paint"[132,133].

After calibration, infrared thermography can be used for temperature measurement and thermal analysis of wide-bandgap semiconductor devices. Reck et al.[134] employed a VarioCAM® high-resolution infrared thermal imager from InfraTec, with a resolution of 1024 × 768 pixels and a thermal resolution better than 0.05 K. Equipped with a macro lens, it provided a spatial resolution of 42–50 μm. Figures 21(a) and (b) show the camera setup and the thermal image of a GaN HEMT. Moultif et al.[135] used an infrared thermal microscope from Quantum Focus Instruments (QFI) to measure the two-dimensional temperature distribution of a multi-finger GaN HEMT. This system was equipped with an InSb 512 × 512 pixel camera, achieving thermal imaging mapping by recording the infrared radiation distribution on the sample surface. At 20× magnification, the spatial resolution of this mode approached 2 μm. Under operating conditions of V_{DS} = 43 V, V_{GS} = 0 V, and P = 43 W, the measured temperature distribution is shown in Figure 21(c). Harris et al.[132] also used the QFI infrared system, as shown in Figure 21(d), to demonstrate the temperature distribution characteristics of a GaN HEMT on a CMOS substrate. In measuring the junction temperature of multi-finger GaN HEMTs, Baczkowski et al.[130] used the QFI infrared microscope system to obtain surface temperature distribution maps under DC bias conditions (Figure 21(e)). This thermal image was captured after the device reached thermal steady state, clearly displaying the temperature field characteristics of the multi-finger structure. Jiang et al.[55] removed part of the packaging material from a SiC MOSFET and directly captured the chip surface temperature distribution using an infrared thermal imager, as shown in Figure 21(f).

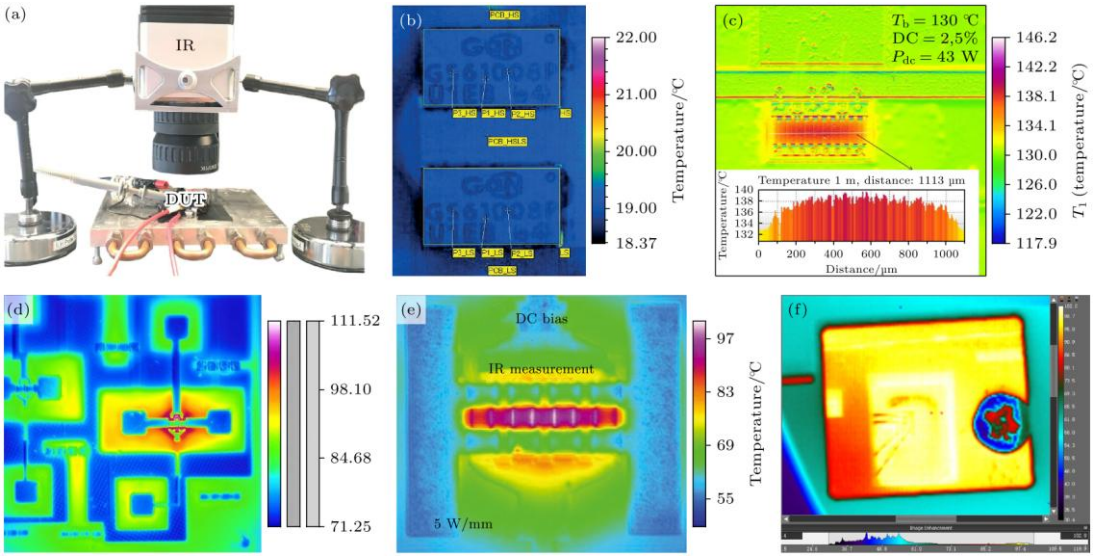


Fig. 21 (a) Schematic diagram of the infrared thermal imaging setup; (b) infrared thermal image of GaN HEMT; (c) temperature distribution map of GaN HEMT obtained by the QFI system at 4× magnification[135]; (d) infrared thermal imaging of GaN HEMT stacked on CMOS[132]; (e) infrared thermal imaging results of GaN HEMT under DC bias[130]; (f) infrared thermal imaging of SiC MOSFET[55].

However, due to the limited spatial resolution of infrared thermography, the directly measured temperature is often significantly lower than the actual junction temperature of the device[128,136-138]. This limitation is particularly pronounced in the thermal characterization of GaN devices with narrow source-drain spacing. The low spatial resolution makes it difficult to accurately resolve the temperature distribution in the device channel region, thereby affecting temperature-based reliability analysis and failure prediction. To reveal the actual maximum junction temperature inside GaN HEMTs, Zafar et al.[139] combined infrared thermography with three-dimensional finite element thermal simulations. The study focused on a two-stage X-band low-noise amplifier (LNA) MMIC, where the first stage employed a 4×50 μm GaN HEMT and the second stage used a 4×75 μm GaN HEMT, with a device spacing of 1.125 mm. Figure 22(a) shows the temperature distributions on the MMIC surface and in the two-dimensional electron gas region obtained from simulations, as well as the temperature distributions measured by infrared thermography using a QFI thermal microscope with 12× magnification. Experimental results showed that the actual peak temperatures of HEMT1 and HEMT2 were 149 ℃ and 145.8 ℃, respectively, whereas the infrared measurements were only 109 ℃ and 108.3 ℃, representing an underestimation of up to 40 ℃.

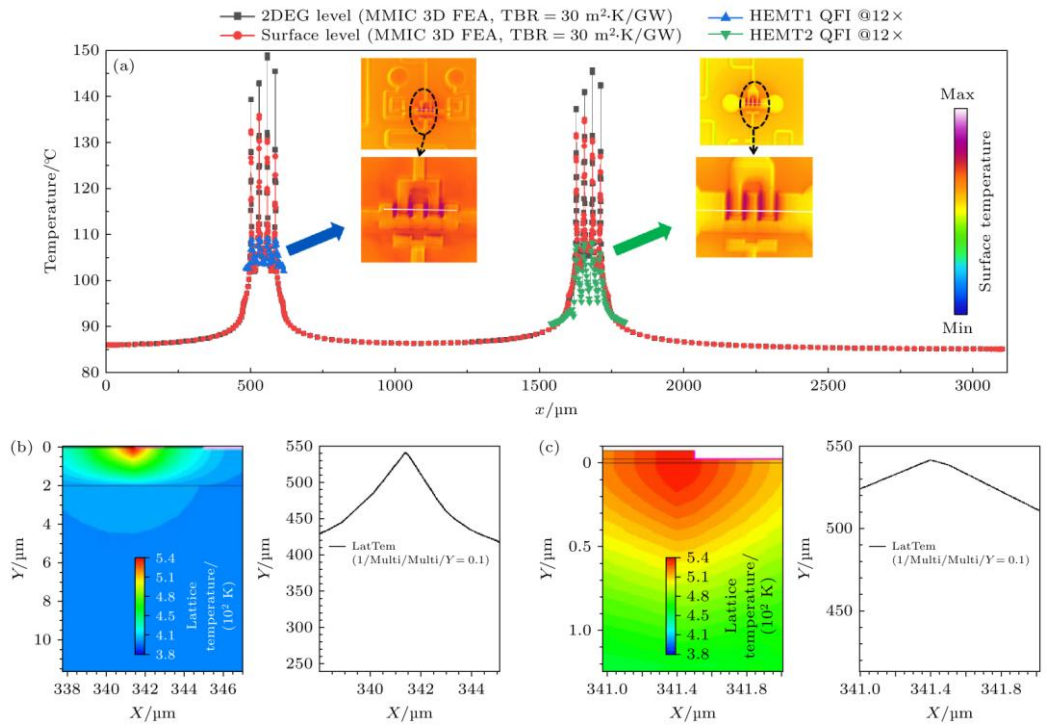


Fig. 22 (a) Comparison of temperature distributions on the GaN HEMT obtained by infrared QFI (12× magnification) and 3D finite element simulation[139]; (b) temperature distribution in a 7 μm region near the gate[140]; (c) temperature distribution in a 1 μm region near the gate[140].

Furthermore, Li et al.[140] combined infrared thermography with Sentaurus TCAD simulations. They investigated GaN HEMT devices with a field-plate structure and a gate length of 0.5 μm. An infrared camera with a spatial resolution of 7 μm measured the chip surface temperature distribution under various power dissipations (2.8—14.0 W). These measurements served as boundary conditions to optimize the TCAD simulation model parameters. Model extrapolation revealed that increasing the resolution from 7 μm to 1 μm raised the maximum junction temperature near the HEMT gate from 197.8 ℃ to 267 ℃ (Fig. 22(b), (c)). This finding highlights the temperature underestimation caused by the spatial averaging effect in infrared measurements. Consequently, inaccurate temperature determinations via infrared thermography in lifetime testing yield unrealistic activation energies[141,142], thereby compromising the accuracy of lifetime predictions. Nevertheless, infrared thermography remains a valuable tool for rapid device comparison and screening, although the peak temperatures determined by this technique require careful interpretation.

4.2 Raman Spectroscopy Thermometry

Raman spectroscopy thermometry is a non-contact temperature measurement technique with high spatiotemporal resolution, based on the principle of inelastic light scattering[142–147]. Its physical basis is the Raman scattering effect. When a laser is

focused onto the material surface through a microscope objective, as shown in Fig. 23(a) and (b), a portion of the scattered light undergoes a frequency shift (Raman shift). This shift is directly related to the intrinsic frequency of lattice vibrations (phonons) in the material. Temperature changes in the material alter the lattice constants and chemical bond strengths through thermal expansion and phonon-phonon interactions. These changes cause systematic shifts in parameters such as the peak position, width, and intensity of Raman characteristic peaks[148–151]. For various wide-bandgap semiconductor materials (such as GaN, SiC, and Ga_2O_3), their characteristic Raman phonon modes (the E_2(high) mode of GaN, the E_2(high) mode of SiC, and the A_{1g}(low) mode of Ga_2O_3) exhibit an approximately linear negative temperature coefficient within specific temperature ranges[142,152,153]. Once this coefficient is precisely calibrated, the local temperature can be derived from the experimentally measured peak shift. During actual measurement, scanning the focused laser spot across the device allows for point-by-point temperature mapping. For instance, lateral scanning in one dimension can measure the channel temperature line profile in GaN HEMTs (Fig. 23(d)), while two-dimensional scanning can obtain the surface temperature distribution of GaN HEMTs (Fig. 23(e))[154,155].

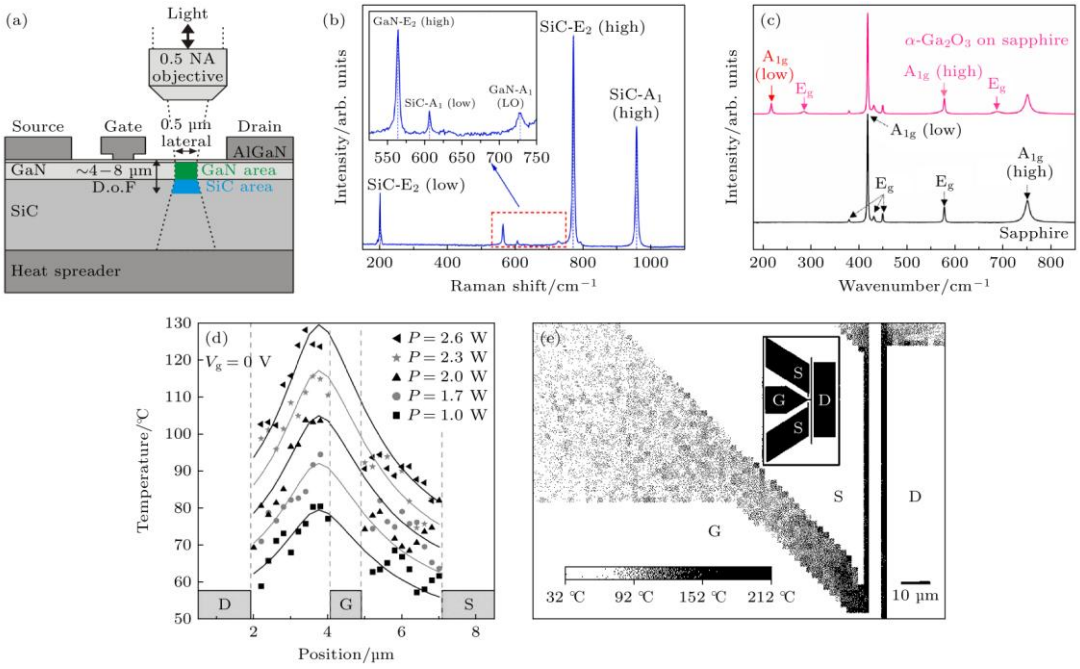


Fig. 23 (a) Schematic diagram of the Raman thermal imaging setup[142]; (b) characteristic Raman peaks of GaN and SiC[153]; (c) Raman characteristic peaks of Ga_2O_3[151]; (d) lateral temperature distribution profiles at different power levels[155]; (e) two-dimensional temperature distribution map of the device[154].

To address the issue of Raman laser blockage by the top metal gate and field plate structures in GaN HEMTs, researchers have developed various innovative optical detection schemes. The first category of schemes bypasses the obstruction by

performing detection from the device backside. Sarua et al.[156] pioneered this approach by establishing an optical path through a double-side polished SiC substrate (Fig. 24(a)). They used a 488 nm sub-bandgap laser to excite Raman signals from the backside, achieving non-destructive temperature measurement of the active region in top-metallized GaN HEMTs with a spatial resolution of 0.5 μm. The measured temperature distributions of the GaN and SiC layers are shown in Fig. 24(b) and (c). However, this method compromises the heat sink, leading to inaccurate device junction temperature readings. The second category involves directly introducing foreign substances with high Raman activity onto the metal surface as temperature probes. The study by Simon et al.[157] is representative; they deposited diamond particles with diameters ≤1 μm on the gate metal surface of GaN HEMTs (Fig. 24(d)). Due to the temperature-sensitive characteristic Raman peak and high thermal conductivity of diamond, the measured temperature rise near the gate deviated from the simulated channel peak temperature by only 10%, as shown in Fig. 24(e). Compared to Raman thermometry targeting the GaN bulk region (which tends to underestimate temperature rise), this method offers greater accuracy. Similarly, Brocero et al.[158] deposited cerium dioxide microparticles on GaN HEMTs via spin coating, enabling simultaneous multi-point temperature measurement of the semiconductor, metal contacts, and GaN bulk region, thereby further expanding the applicability of this method. The third category adopts a multi-physics fusion approach. Instead of directly detecting the blocked area, it infers temperature through correlated measurements. Kim et al.[159] combined Raman thermal imaging with gate resistance thermometry: Raman spectroscopy precisely measures the temperature distribution in optically accessible regions, while the resistance change of the gate metal reflects the average temperature of the hotspots beneath it (Fig. 24(f)). By integrating both datasets with a thermal model, the deviation between the inferred channel peak temperature and the model prediction was less than 4% under fully on-state conditions for GaN HEMTs, providing a high-precision validation method for indirectly obtaining peak temperatures.

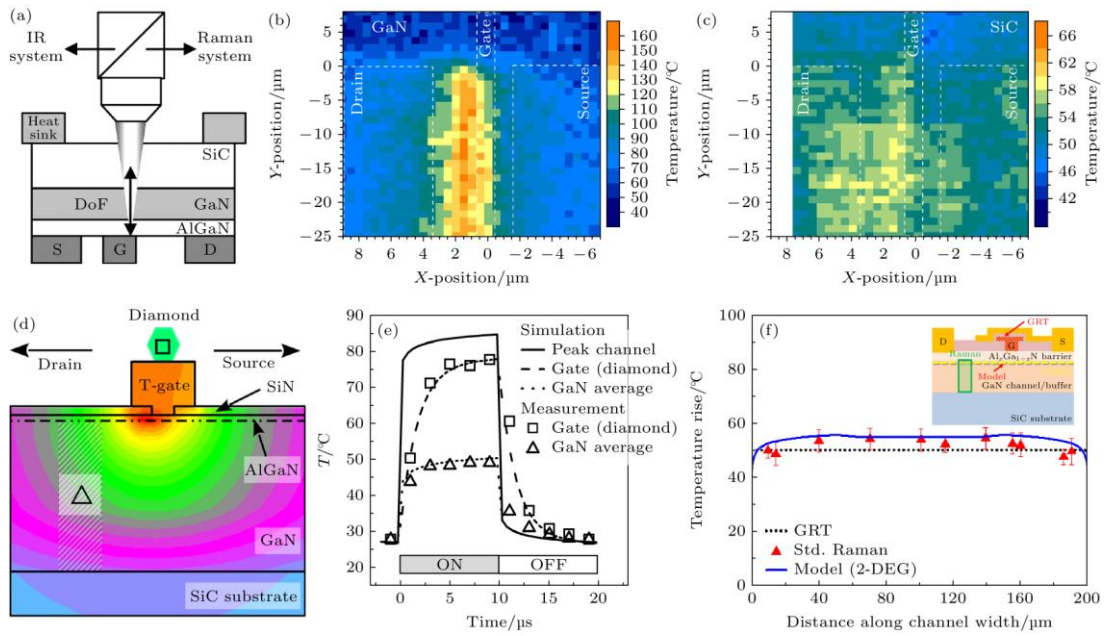


Fig. 24 (a) Schematic diagram of the device structure and experimental setup[156]; (b) temperature distribution map of the GaN layer measured by Raman spectroscopy[156]; (c) temperature distribution map of SiC measured by Raman spectroscopy[156]; (d) cross-sectional structure of the GaN HEMT and finite element simulation temperature contours. Diamond particles are deposited above the gate[157]; (e) transient temperature of the GaN region and the diamond particles above the gate, along with the simulated transient curve of peak channel temperature[157]; (f) temperature rise distribution along the channel width under fully-on conditions; the inset shows the measurable temperature rise locations for each experimental method[159].

Beyond steady-state measurements, characterizing the transient thermal behavior of devices under pulsed operation is equally critical. This necessity has driven the development of time-resolved micro-Raman techniques. The core of this technology involves using an acousto-optic modulator (AOM) or an electro-optic modulator (EOM) to modulate a continuous-wave laser into a narrow pulse sequence synchronized with electrical pulses. Kuball et al.[160] developed time-resolved micro-Raman thermography, as shown in Figure 25(a). In this study, an AOM modulated a 488 nm argon-ion laser into a pulse sequence with a 200 ns pulse width. Combined with programmable delay control, this setup achieved precise synchronization between pulsed biasing and optical probing. The system achieved a spatial resolution of 0.5-0.7 μm and improved the temporal resolution to 200 ns. As shown in Figures 25(b) and (c), the peak temperature of the GaN HEMT is located in the gate-drain region. Within a 2 μs pulse, the temperature rise occurs primarily during the first 1 μs. Fan et al.[153] developed a novel opto-electrical flash Raman method. The measurement system established in this study is shown in Figure 25(d). An EOM modulates the continuous-wave laser into probing pulses, while a scanning galvanometer controls

laser focusing. A grating and a CCD are used to resolve the Raman spectrum. Figure 25(e) compares the temperature response of GaN HEMTs under different driving frequencies. At 100 Hz, the single-cycle temperature difference in the GaN active layer reaches 26 K, whereas the SiC substrate exhibits smaller fluctuations, indicating thermal transfer delay. At 1000 Hz, the temperature fluctuation range decreases to 8 K, but the average operating temperature rises significantly. This indicates that high-frequency operation increases the steady-state temperature of the device. Bagnall et al.[161] used an AOM to modulate a 532 nm continuous-wave laser into a pulse sequence with a 30 ns pulse width. Combined with synchronized electrical pulse biasing (minimum pulse width of 200 ns), they achieved a transient temperature measurement system with a temporal resolution of 30 ns. For gateless GaN HEMT devices, the system measured temperature responses corresponding to different pulse widths ranging from 12.5 to 50 μm under a power dissipation of 20 W/mm. This process constructed a complete temperature response curve, as shown in Figure 25(f). Riedel et al.[162] used an AOM to modulate a 532 nm laser into a pulse sequence with a pulse width of 10-15 ns. Combined with synchronized electrical pulse biasing (200 ns pulse width, 10 ns rise/fall time), they improved the temporal resolution to the 10 ns level for the first time, while maintaining a spatial resolution of 0.5-0.7 μm. They obtained the temperature evolution of gateless GaN HEMT devices grown on SiC and sapphire substrates. The study found that within 70 ns after device turn-on, the temperature rise curves for devices on SiC and sapphire substrates differ little, as shown in Figure 25(g). This indicates that thermal dynamics in this stage are dominated by the thermal parameters of the GaN layer, and the difference in substrate thermal conductivity has not yet exerted an influence. After 70 ns, the temperature rise rate of the device on the SiC substrate slows down significantly due to its high thermal conductivity.

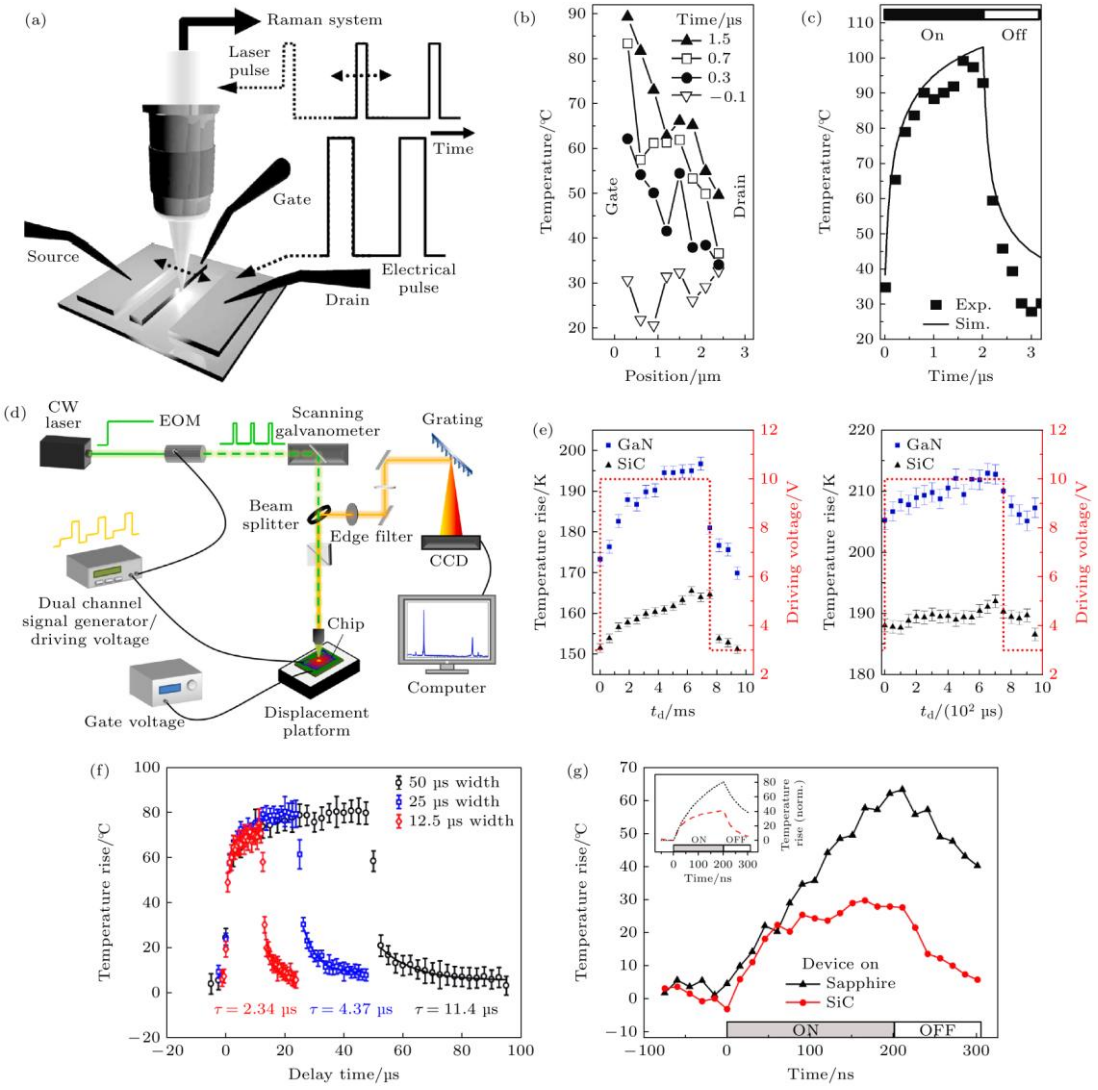


Fig. 25 (a) Schematic of the time-resolved micro-Raman thermography setup[160]; (b) temperature distribution profiles in the gate-drain region at different time points[160]; (c) evolution curve of the peak temperature over time[160]; (d) schematic diagram of the optoelectronic flash Raman measurement system[153]; (e) temperature variations of GaN and SiC under modulation signals at 100 Hz and 1000 Hz[153]; (f) transient temperature rise curves of the GaN HEMT under different pulse widths[161]; (g) temperature variation curve over time at the center of the device for gate-free GaN HEMTs based on SiC and sapphire substrates, with thermal simulation results shown in the inset[161].

Karim et al.[151] employed micro-Raman spectroscopy to measure the junction temperature of α-Ga_2O_3 MOSFETs. They excited the A_{1g}(low) phonon mode of α-Ga_2O_3 (wavenumber approximately 217 cm^{-1}) using a 532 nm laser. Temperature measurements relied on the quantitative relationship between temperature and both peak shift and spectral line broadening. As shown in Fig. 26(a), the temperatures measured by two Raman methods align closely with three-dimensional thermal simulation results within a power density range of 1-5 W/mm (deviation <8%). Notably,

under low-power conditions (1-3 W/mm), the temperature difference between the peak-shift-based measurements and simulations is only 1-3 ℃. However, under high-power conditions (4-5 W/mm), this method underestimates the temperature by 5-10 ℃. This deviation is attributed to compressive stress effects generated during device operation. Pomeroy et al.[163] deposited 30 nm titanium dioxide nanoparticles on the surface of β-Ga_2O_3 MOSFETs as temperature probes. They excited the Raman signals using a 488 nm argon ion laser. Fig. 26(b) presents the temperature distribution along the channel direction (from gate to drain) under a drain-source voltage of 50 V (power dissipation density 1.87 W/mm). The measurement results show high agreement with simulations, with a maximum temperature difference not exceeding 12 ℃.

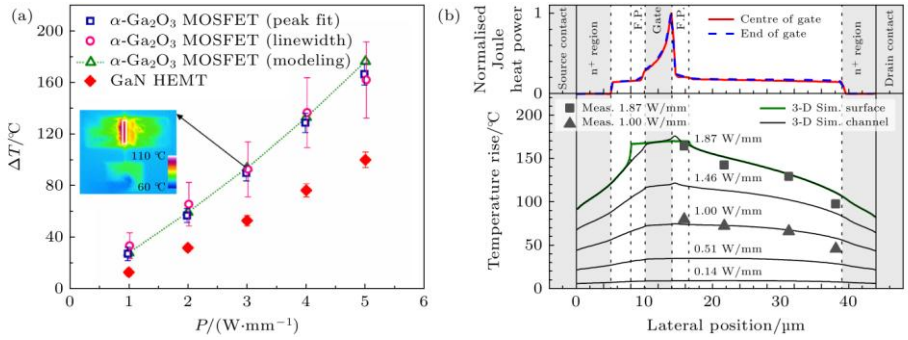


Fig. 26 (a) Channel temperature rise versus power density of the α-Ga_2O_3 MOSFET; the inset shows infrared thermography[151]; (b) normalized simulated Joule heating power distribution obtained from the two-dimensional drift-diffusion model (top), and comparison of temperature rise between Raman measurements and simulated predictions (bottom)[163].

It is particularly important to note that for wide-bandgap semiconductor devices, such as gallium nitride (GaN), internal energy dissipation and heat transfer constitute a multi-stage, non-equilibrium dynamic process[164,165]. Infrared thermography and Raman spectroscopy primarily detect signals originating from optical phonons within lattice vibrations. Consequently, the directly measured temperature approximates the optical phonon temperature. However, Joule heat generated within the device must ultimately conduct to the heat sink via acoustic phonons. Under high power density conditions, particularly during pulsed operation, instantaneous thermal equilibrium among electrons, optical phonons, and acoustic phonons may not be achieved. This results in the optical phonon temperature exceeding the acoustic phonon temperature, indicating a significant state of thermal non-equilibrium[166,167]. This non-equilibrium state implies that the "apparent" temperature directly measured by infrared or Raman techniques (excluding other error sources) may exceed the average junction temperature or acoustic phonon temperature of the device. Therefore, this discrepancy requires careful consideration when evaluating maximum junction temperature,

thermal resistance, and reliability predictions. Future thermal management designs must develop multi-scale models capable of distinguishing and coupling these different heat carriers to achieve more precise thermal analysis and optimization.

4.3 Thermoreflectance Technique

Surface reflectivity exhibits temperature dependence[168-170]. Unlike Raman scattering, optical reflection involves incident and reflected photons of identical wavelength, but the intensity of the reflected photons depends on temperature. The relative change in optical reflectivity with temperature is minimal[143], typically on the order of 10^{-5} to 10^{-4} K^{-1}. Depending on the detection method, thermoreflectance techniques are primarily categorized into single-point temperature measurement and full-field temperature imaging.

Single-point temperature measurement typically employs a low-repetition-rate laser (typically below 30 kHz) as the pump source and a continuous-wave laser as the probe beam. The typical system configuration is shown in Figure 27(a)[122,171,172]. The selection of probe wavelength directly influences the measurement target and accuracy. Photons with energy slightly higher than the semiconductor bandgap can penetrate surface metal and dielectric passivation layers and are strongly absorbed within the semiconductor layer, enabling direct detection of channel temperature. In contrast, visible light (e.g., 532 nm) or near-infrared light is primarily used to measure the temperature of surface metal electrodes[173,174]. The signal representing reflectivity changes over time induced by the pump pulse sequence (i.e., the time-domain thermoreflectance transient signal) is monitored by the continuous-wave laser and directly acquired via an amplified photodetector and a digital oscilloscope. Figure 27(b) illustrates the typical morphology of the time-domain thermoreflectance transient signal detected under pulsed heating[122]. The time resolution is primarily determined by the pump pulse width and detector response speed, easily reaching the picosecond to nanosecond range. To achieve two-dimensional temperature distribution imaging, such systems must be combined with high-precision scanning galvanometers or sample displacement stages to acquire spatial information through point-by-point scanning.

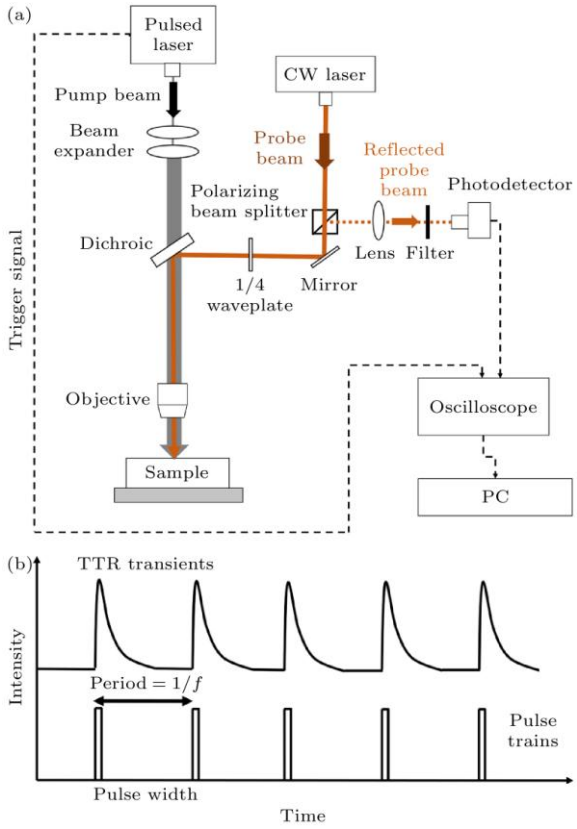


Fig. 27 (a) Schematic diagram of the transient thermoreflectance measurement setup[122]; (b) schematic diagram of a typical transient thermoreflectance signal waveform captured by an oscilloscope[122].

Currently, this technology is widely applied to predict junction temperatures in GaN HEMT devices. Figure 28 presents the results obtained by Helou et al.[175] using thermoreflectance technology based on a 365 nm sub-bandgap excitation light source. They measured temperatures in the channel regions of GaN HEMT devices fabricated on different substrate materials (Si, SiC, and Diamond). The figure displays the average temperature across the entire channel region and the peak temperature within the region under various power densities. The results indicate that devices using SiC substrates exhibit the lowest channel peak temperature at the same power density. This outcome is primarily attributed to the high interfacial thermal resistance at the GaN/Diamond interface. Its adverse effects partially offset the advantage of the high thermal conductivity inherent to the Diamond substrate.

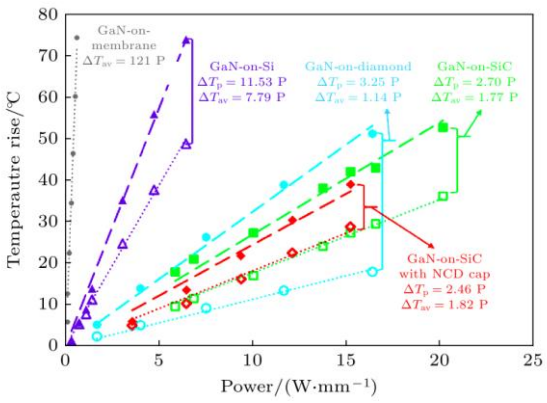


Fig. 28 Average temperature rise (hollow markers) and peak temperature rise (solid markers) in the effective channel region of GaN HEMT devices fabricated on different substrates[175].

Thermoreflectance measurements can also be performed from the device backside, thereby evaluating optically inaccessible metal regions. Martin-Horcajo et al.[176] demonstrated this measurement on a GaN HEMT with a source field plate (Fig. 29(a)). In this measurement, a laser with a wavelength of 530 nm and energy below the bandgaps of GaN and SiC served as the probe light source. It passed through the SiC substrate and AlGaN/GaN layers before focusing on the gate metal (position A). Under pulsed bias conditions (V_{GS} = -3-0 V, period 25 μs, duty cycle 55%), the top-side thermoreflectance signal (position B) and Raman temperature rise data were acquired synchronously. As shown in Fig. 29(b), the channel temperature rise measured by the backside thermoreflectance technique closely matched the finite element simulation results. In contrast, the Raman measurement underestimated the channel temperature rise by approximately 9% without temperature extrapolation. Furthermore, the temperature obtained using the standard front-side thermoreflectance method was only about half of the actual gate metal temperature, indicating a significant underestimation in this structure. Mao et al.[177] developed a multi-wavelength laser transient thermoreflectance (MWL-TTR) technique, with the setup shown in Fig. 29(c). This method employed a 320 nm continuous-wave laser to probe the channel temperature and a 532 nm laser to monitor the metal contact temperature. A high-magnification objective lens (20× UV, NA = 0.38) achieved sub-micron spatial resolution (0.8 μm), while a photodetector with 400 MHz bandwidth provided nanosecond-level temporal resolution. The study quantitatively analyzed the photocurrent effect induced by the 320 nm above-bandgap laser for the first time. For GaN HEMT devices on sapphire substrates, transient temperature rise curves were measured under pulsed bias conditions (V_{GS} = -3.4-3 V, duty cycle 50%) at different pulse widths (Fig. 29(d), (e)).

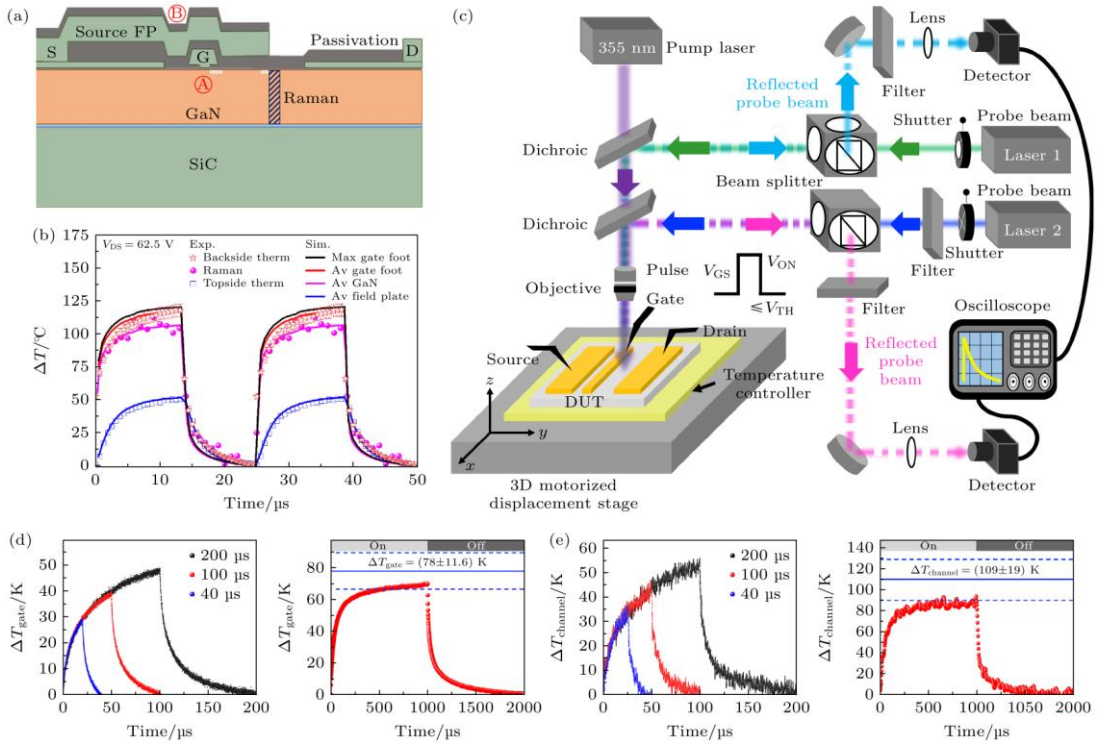


Fig. 29 (a) Cross-sectional schematic of a GaN HEMT, indicating the GaN layer measurement area for Raman thermography; positions A and B are the backside and frontside thermoreflectance measurement points, respectively[176]; (b) temperature versus time at different device locations, the GaN layer, gate foot metal, and source field plate surface above the gate contact[176]; (c) MWL-TTR measurement system[177]; (d) gate temperature versus time under different pulse periods[177]; (e) channel temperature versus time under different pulse periods[177].

Full-field temperature imaging technology is typically implemented using CCD sensors. The general system architecture is shown in Figure 30(a). LEDs serve as illumination sources to irradiate the test sample surface, while CCDs detect the reflection intensity that varies with temperature, thereby achieving full-field temperature imaging[178]. By synchronizing the delay among LED pulses, pulsed excitation of the device under test, and CCD exposure, high-speed transient measurements can be achieved. The time resolution depends on the LED pulse width and can reach an optimal value of 50 ns[179]. TTI has been employed to measure the junction temperature of GaN HEMTs. Tadjer et al.[180,181] utilized a TTI system to evaluate the thermal performance of Si-substrate GaN HEMTs and substrate-free GaN HEMTs. The temperature distributions under different bias conditions are shown in Figure 30(b). Under the same power dissipation, the peak temperature of the substrate-free structure is more than three times higher than that of the Si-substrate structure. Pavlidis et al.[182] achieved temperature distribution measurements for both the GaN channel and the metal gate by using a 530 nm wavelength LED to probe the metal gate and a 365 nm wavelength LED to probe the GaN channel. The

dual-wavelength TTI measurement results are shown in Figure 30(c).

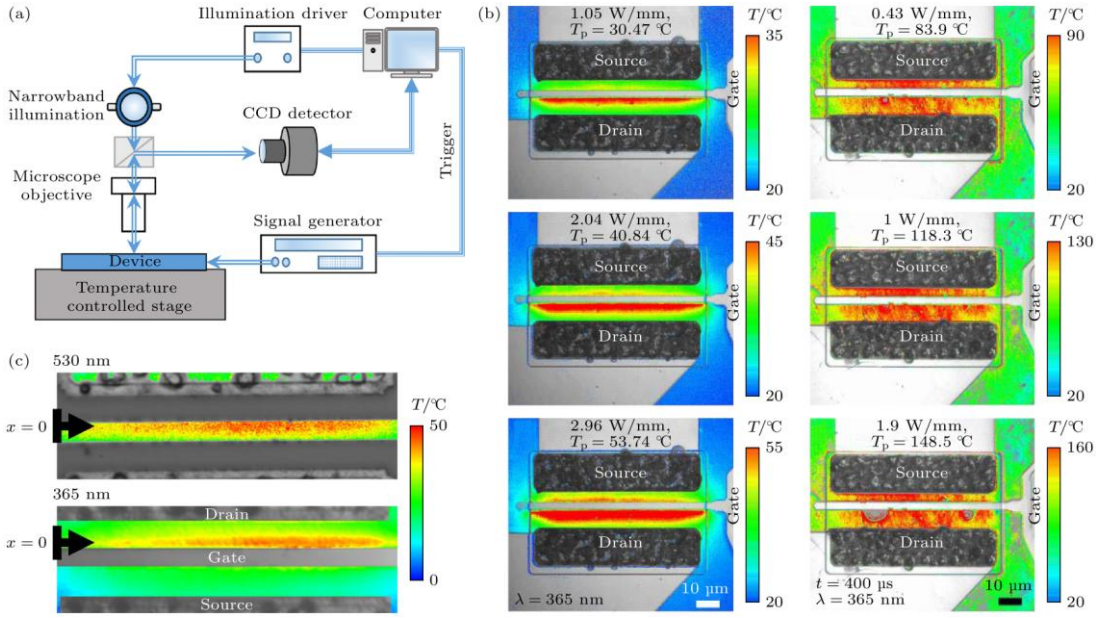


Fig. 30 (a) Schematic diagram of the thermoreflectance measurement configuration[178]; (b) transient thermoreflectance imaging under different electrical conditions[180]; (c) thermoreflectance images obtained using a 530 nm LED (gate metal) and a 365 nm LED (GaN channel), respectively[182].

Furthermore, Liu et al.[183] developed a pulsed thermoreflectance imaging (PTI) method. This approach applies pulsed current excitation to a metal heating line (Au/Cr, 5 μm wide), as shown in Fig. 31(b). It combines dual-wavelength LED illumination sources at 365 nm (for GaN detection) and 530 nm (for Au detection), as illustrated in Fig. 31(c). A CCD thermoreflectance imaging system records the temporal temperature evolution across different spatial regions of the sample surface, as depicted in Fig. 31(a). By precisely controlling the pulse width (0.8—10 μs) and synchronization delay, transient temperature curves (ΔT_1—ΔT_4) are acquired from four characteristic regions (I—IV), as shown in Fig. 31(d)—(f). Multiparameter decoupling is achieved through inversion calculations combined with three-dimensional finite element simulations.

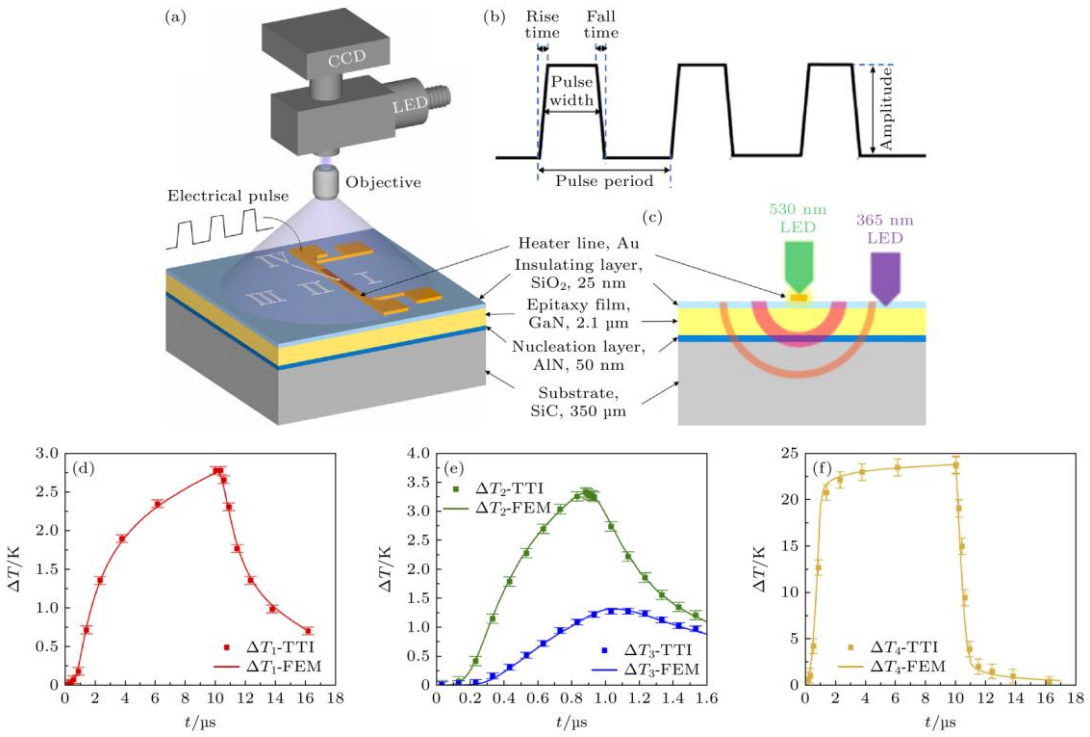


Fig. 31 (a) TTI measurement system[183]; (b) schematic diagram of the applied pulse excitation[183]; (c) pulses of different frequencies applied to the DUT, with different illumination sources used for regions I-IV (Au: 530 nm, GaN: 365 nm); transient temperatures of (d) region I, (e) regions II and III, and (f) region IV; the scatter points represent raw TTI data, and the curves show fitting results based on the 3D finite element method[183].

Lundh et al.[184] employed TTI technology to precisely measure the channel temperature of β-Ga_2O_3 heterojunction field-effect transistors (HFETs). Figure 32(a) presents a micrograph of the β-Ga_2O_3 HFET structure, with arrows indicating the extraction locations for temperature distribution profiles. Figures 32(b) and (c) display the thermoreflectance temperature distributions for the ohmic contact metal and the semiconductor channel region, respectively. The study revealed that both the metal electrodes and the semiconductor channel exhibited significant thermoreflectance responses, with consistent temperature distribution trends. By comparing temperature responses under different pulse widths (600 μs—100 ms) (Figure 32(d)), the researchers confirmed that temperature variation is the dominant factor in thermoreflectance signals, thereby excluding interference from electric field or carrier effects. Chatterjee et al.[185] used TTI technology to compare the peak temperature rise of metal electrodes in Ga_2O_3 and SiC SBDs at identical volumetric power densities (~10 kW/cm^3). As shown in Figure 32(e), due to the lower thermal conductivity of Ga_2O_3 (11—27 W/(m·K)), the peak temperature of its metal electrodes was approximately 67% higher than that of SiC diodes.

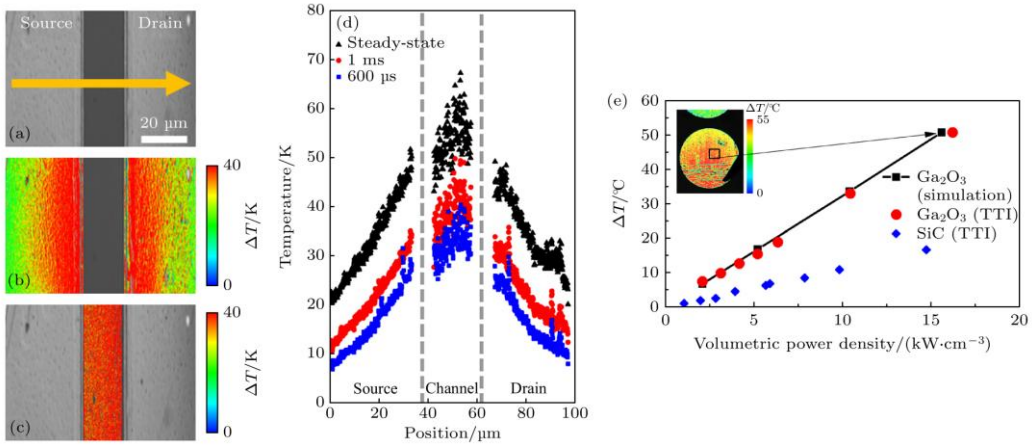


Fig. 32 (a) *β*-Ga_2O_3 HFET structure[184]; temperature rise diagrams of (b) ohmic contact and (c) semiconductor channel[184]; (d) temperature rise curves along the channel length of *β*-Ga_2O_3 HFET structure corresponding to different pulse widths[184]; (e) temperature rise results of metal electrodes in Ga_2O_3 and SiC SBD obtained by TTI[185].

4.4 Quantum Sensing Technology

Quantum sensing technology leverages the sensitivity of quantum states in solid-state defect centers to external physical quantities, such as temperature, magnetic fields, and electric fields. This approach provides a novel pathway for achieving nanoscale, high-precision measurements[186-188]. Currently, this technology remains primarily in the basic research stage. It has not yet matured into established applications for the direct junction temperature measurement of wide-bandgap semiconductor devices. Nevertheless, its unique performance metrics, including non-contact operation, high precision, and multi-parameter sensing, indicate significant potential for reliability design and online monitoring of wide-bandgap semiconductor devices.

The nitrogen-vacancy (NV) center in diamond is the most extensively studied quantum sensing platform. The splitting of its electronic spin ground state under zero magnetic field is sensitive to temperature, enabling thermometry via optically detected magnetic resonance (ODMR)[189,190]. Zhang et al.[191] developed a fiber-integrated NV quantum thermometer. By tracking peak structures in the zero-field ODMR spectrum, they effectively isolated interference from magnetic fields and microwave power drift. This method achieved a sensitivity of 18 mK/$\sqrt{\text{Hz}}$ in surface temperature imaging of electronic chips (Fig. 33(a)–(c)). However, the study did not explicitly specify that the electronic chips used were wide-bandgap semiconductor devices. Gong et al.[192] further enhanced the temperature response of NV centers using gadolinium flux enhancement. They improved the sensitivity to 251.5 nK/ $\sqrt{\text{Hz}}$ under near-room-temperature conditions. They also noted the need to address interface thermal resistance and electromagnetic compatibility issues associated with integration into semiconductor devices.

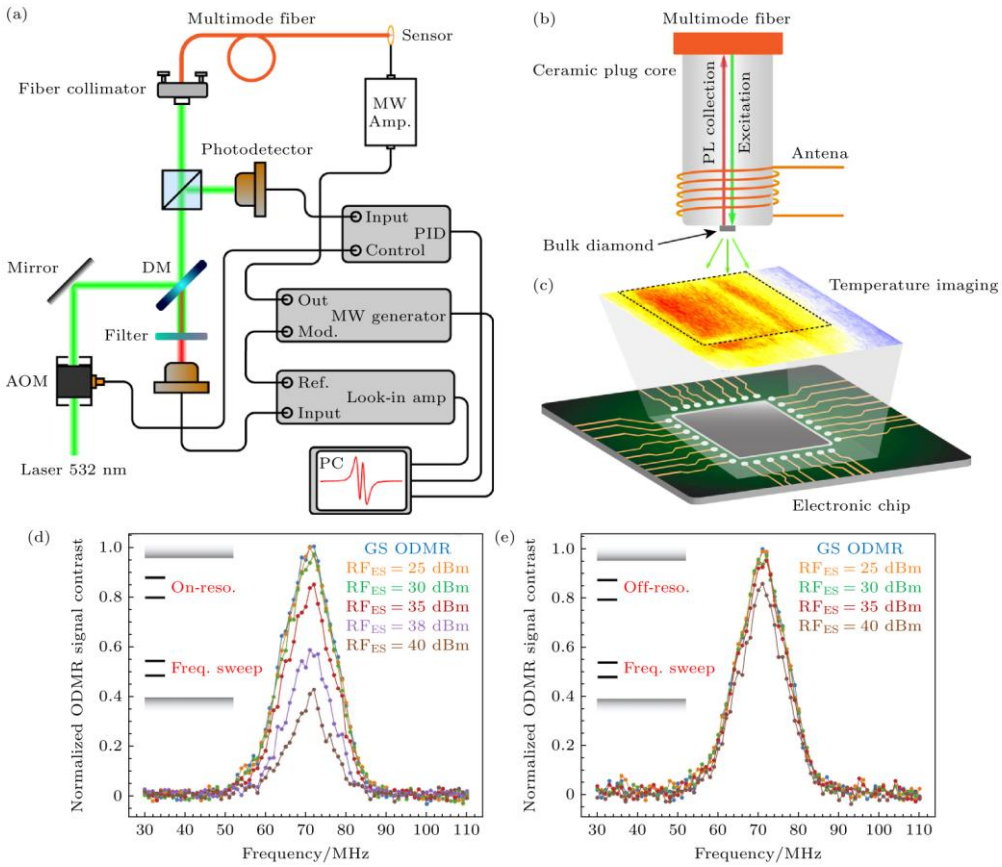


Fig. 33 (a) Schematic diagram of the hybrid fiber thermometer device[191]; (b) simplified schematic of the sensor[191]; (c) chip for temperature imaging based on fiber-optic quantum thermometers[191]; evolution of optically detected magnetic resonance of off-resonance in the excited state from (d) 410 MHz and (e) 300 MHz [193].

As a mature semiconductor material, silicon carbide (SiC) features vacancy defects, such as silicon vacancies, that combine optically addressable spins with telecom-band emission advantages. These characteristics facilitate monolithic integration with SiC power devices. Addressing the challenge of temperature-insensitive ground states in silicon vacancies, Yamazaki et al.[193] proposed a synchronized optically detected magnetic resonance (ODMR) method, as shown in Fig. 33(d) and (e). By simultaneously driving ground-state and excited-state resonances, this approach transfers part of the ground-state ODMR contrast to temperature measurement, enhancing signal intensity by an order of magnitude. Within a range of 400 K, the thermal drift reaches 1.3 MHz/K. This method is theoretically suitable for internal temperature mapping of SiC devices, although it has not yet been validated for actual junction temperature monitoring. Tahara et al.[194] leveraged the spin properties of silicon vacancies to develop duplex qubit operations. By simultaneously driving multiple transition pairs, they doubled the ODMR contrast, achieving an AC magnetometry sensitivity of 1.4 $\mu T/\sqrt{Hz}$. While this design resists device current noise, it requires optimized surface passivation to reduce interface defect interference. Jiang et

al.[195] realized radio-frequency signal quantum sensing of silicon vacancies in SiC. They extended the coherence time to 28.1 μs via dynamic decoupling and achieved a spectral resolution of 10 kHz at a frequency of 900 kHz. Synchronous readout techniques further improved the resolution to 0.01 kHz, laying the foundation for detecting high-frequency thermal fluctuations in junction temperature monitoring.

In summary, infrared thermography is currently the most widely used method for temperature measurement in wide-bandgap semiconductor devices due to its non-contact, full-field, and rapid imaging capabilities[196,197]. Its core advantage lies in the direct acquisition of two-dimensional temperature distributions within a mesoscopic field of view, typically ranging from several micrometers to millimeters[198]. However, infrared measurement accuracy faces fundamental challenges for devices with complex multilayer structures, such as metal interconnects, dielectric layers, and semiconductor heterojunctions. First, the emissivity of different materials on the device surface, such as GaN, metal electrodes, and SiN passivation layers, is difficult to calibrate precisely. Furthermore, emissivity varies with wavelength, temperature, and surface morphology. This variation is the primary cause of significant underestimation of hotspot temperatures, with errors sometimes exceeding 50%[199]. Second, the diffraction limit of infrared light restricts its ability to resolve spatial details of sub-micron hotspots. Additionally, lateral thermal diffusion blurs hotspot regions and smooths temperature gradients in infrared images. Raman thermography and thermoreflectance techniques, as optical methods with higher spatial resolution (reaching sub-micron scales or even below the diffraction limit), have become powerful tools for nanoscale thermal analysis[200,201]. They provide temperature analysis with extremely high spatial and temporal resolution. However, Raman technology has limitations. Laser irradiation may cause local photothermal heating, particularly in materials with low thermal conductivity. Metal layers, such as field plates, strongly absorb or reflect laser light, interfering with signal acquisition. Raman shifts are influenced by both temperature and stress. Decoupling these factors requires complex calibration and multi-peak analysis, which is rigorous and time-consuming. As Raman technology is essentially a point-scanning technique, its imaging speed is much slower than that of infrared global imaging[202]. Thermoreflectance technology is highly sensitive to the optical properties and flatness of the sample surface. Interference effects from dielectric film layers or nanoscale changes in surface roughness can introduce significant signal-to-noise ratio degradation and measurement errors.

5 Conclusion and Outlook

5.1 Summary

This paper systematically reviews and evaluates mainstream technologies for junction

temperature measurement in wide-bandgap semiconductor devices, covering electrical, physical contact, and optical methods. Table 2 compares the characteristics of these three categories of junction temperature extraction methods. No single technology can independently meet the composite requirements of high spatial resolution, high temporal resolution, high accuracy, non-invasiveness, and full-field imaging for wide-bandgap semiconductor devices[203-205]. The core advantage of electrical methods based on temperature-sensitive parameters is their ability to perform non-destructive online and in-situ monitoring. They are particularly suitable for lifetime testing and system status monitoring of packaged devices. Their main disadvantages include low spatial resolution, as they measure spatially averaged temperatures, and susceptibility to interference from device aging, electrical stress, and measurement circuit noise. Errors primarily stem from the calibration accuracy of temperature-sensitive parameters and non-thermal changes in the device itself. The typical error range is approximately ±5-±15 ℃ or higher, and errors may expand further under extreme or dynamic operating conditions. Physical contact methods provide high spatial resolution and direct physical temperature measurement. On-chip integration methods can achieve true in-situ, real-time junction temperature monitoring. However, their inherent disadvantage is the potential introduction of contact thermal resistance, which interferes with the measured temperature field. Scanning thermal microscopy is slow and requires a vacuum environment, while on-chip integrated thermal sensors require additional specialized processes, altering device structure and cost. Errors are mainly determined by the quality of thermal contact between the sensor and the measurement point, the self-heating effect of the sensor, and the accuracy of the readout circuit. The ideal error for on-chip integrated thermal sensors can be as low as ±1-±5 ℃. As a representative of non-contact measurement, optical methods provide excellent spatial resolution (micrometer to sub-micrometer scale) and thermal distribution maps. They are the gold standard for analyzing hotspots, failure mechanisms, and validating thermal models. Their limitations include the need for optical access (which may require decapsulation), strong dependence on material optical properties (such as emissivity and Raman scattering cross-section), and expensive, complex equipment. Errors mainly arise from emissivity calibration errors, the diffraction limit of optical systems, and peak shifts caused by mechanical strain. With careful calibration, the absolute error of micro-Raman and thermoreflectance methods can be controlled within ±3-±10 ℃, while the error of infrared cameras for un-decapsulated devices may exceed ±10 ℃.

Table 2. Comparison of characteristics among three junction temperature extraction methods.

Method		Global imaging	In-situ on-line capability	Time resolution	Spatial resolution	Accuracy	Cost	Complexity
Electrical method		No	Yes	ns—μs	—	Low	Low	Yi
Physical contact method	Scanning thermal microscope	Yes	No	ms	μm—mm	High	Medium	Medium
	Thermocouple/thermal resistance	No	No	ms	μm—mm	Medium	Medium	Medium
	Integrated nonlinear element	No	Yes	ms	—	High	High	Difficult
Optical method	Infrared thermography	Yes	No	10 μs	3—10 μm	Medium	High	Medium
	Raman spectrum	Yes	No	10 ns	0.5—1 μm	High	Extremely high	Difficult
	Heat reflection	Yes	No	10 ns	0.5—1 μm	High	Extremely high	Difficult

Method selection should adhere to the following principles. Electrical methods are preferred for large-scale production line testing or online health management of packaged devices due to their convenience and low cost. Optical methods are indispensable for device development, failure analysis, or microscopic thermal distribution studies. Infrared thermography is recommended when thermal map visualization or rapid verification is required. Raman spectroscopy or thermoreflectance is prioritized for precise channel temperature measurement, microscopic material temperature analysis, or research validation. Physical contact methods, particularly on-chip integration strategies, should be employed for highest-precision point measurements or thermal characterization of advanced nanodevices, provided that corresponding fabrication and testing conditions are available.

5.2 Future Challenges

As wide-bandgap semiconductor devices evolve toward higher frequencies, higher power densities, smaller dimensions (such as nanoscale gate lengths), and more complex integration (such as 3D heterogeneous integration)[206,207], precise junction temperature measurement faces increasingly severe challenges.

1) Measurement limits under dynamic and extreme conditions: Future 6G communication and power switching applications require capturing ultrafast transient thermal processes at the nanosecond or even sub-nanosecond scale. They also demand precise synchronous measurement in environments with high electromagnetic interference and high-voltage isolation. These requirements impose near-limit demands on the time resolution, synchronous triggering accuracy, and anti-interference capability of measurement systems. Furthermore, the scaling of device feature sizes reduces the physical scale of hotspots to the sub-micron or even nanometer range. Achieving high spatial resolution matching these scales under dynamic conditions presents a systematic challenge to existing technical frameworks.

2) Characterization of three-dimensional and buried thermal distributions: Three-dimensional integration, vertical structure devices, and channels covered by

thick field plates, multi-layer metals, and passivation layers cause key heat sources to be deeply buried. Obtaining the three-dimensional temperature field distribution inside devices non-destructively and in situ, rather than merely surface or two-dimensional projections, represents a major bottleneck for existing technology systems primarily based on surface detection.

3) Signal decoupling under strong multi-physics coupling: Under real operating conditions, electric, thermal, and stress fields are strongly coupled[208-211]. Changes in temperature measurement signals often represent mixed responses from trap effects, thermal effects, and stress effects. High-fidelity decoupling of pure thermally induced components from complex temperature measurement signals constitutes a fundamental challenge for various thermometry methods.

5.3 Outlook

To address the aforementioned challenges, future junction temperature measurement technologies for wide-bandgap semiconductor devices will exhibit a trend toward multi-dimensional and cross-scale collaborative development.

1) Multi-technology fusion and inversion reconstruction: The limitations of single technologies will drive the formation of multi-physics and multi-technology collaborative measurement paradigms. For instance, combining optical thermometry with high spatiotemporal resolution, in situ electrical thermometry, and artificial intelligence models can construct a collaborative "thermal-electrical-mechanical" measurement paradigm. This approach enables a leap from local point measurements to full-field three-dimensional reconstruction, and from indirect inversion to intelligent prediction.

2) Deep structure characterization technologies: Emerging technologies such as X-ray nanodiffraction and terahertz time-domain spectroscopy will see wider application to meet the measurement needs of multi-layer packaging and deeply buried heat sources. In particular, synchrotron radiation X-ray technology can achieve indirect temperature inversion and characterization of deeply buried interfaces and three-dimensional structures inside devices. This provides new pathways for solving temperature measurement problems in “black box” style packaging.

3) Quantum precision sensing technologies: Quantum sensing systems, represented by diamond nitrogen-vacancy centers and quantum dots, will drive thermometry technologies toward atomic-scale resolution and millikelvin-level sensitivity. These technologies not only enable precise localization and temperature imaging of nanoscale heat sources but also simultaneously acquire multi-physics information such as local magnetic fields and strain. They provide revolutionary tools for studying multi-coupling mechanisms such as thermal-electrical-mechanical interactions in GaN devices.

In conclusion, the development of precise junction temperature measurement technologies for wide-bandgap semiconductor devices holds irreplaceable core value for revealing microscopic heat generation and dissipation mechanisms, predicting device lifetime, and guiding high-reliability design. This direction urgently requires deep interdisciplinary integration involving physics, thermodynamics, microelectronics, optics, quantum sensing, artificial intelligence, and materials science. It also requires pooling the collective wisdom of academia and industry to break through current technical bottlenecks. This will provide solid experimental support and scientific foundation for developing wide-bandgap semiconductor devices with higher power density, higher operating frequency, and longer lifespan.

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