Research progress on scaling technology of amorphous Indium Gallium Zinc Oxide Thin-Film Transistors*

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Abstract

In the post-Moore era, oxide thin-film transistors (TFTs), particularly wide-bandgap semiconductor transistors represented by amorphous indium gallium zinc oxide (a-IGZO), have attracted significant attention due to their low-temperature fabrication process, excellent compatibility with back-end-of-line (BEOL) processes, and outstanding electrical performance. These devices have been widely applied in fields such as displays, monolithic three-dimensional (3D) integration, and memory technologies. This article focuses on the dimensional scaling technology of a-IGZO TFTs, especially two key dimensions—channel length (L_{ch}) and contact length (L_C)—to enhance density and performance. For channel scaling, architectural innovations such as dual-gate structures have been instrumental in mitigating short-channel effects, enabling devices with L_{ch} scaled down to 30 nm to achieve a near-ideal subthreshold swing of 63.4 mV/decade and a high transconductance of 559 μS/μm. Concurrently, vertical transistor designs, like channel-all-around architectures, have successfully pushed L_{ch} to 50 nm while maintaining excellent gate control and leakage currents below 10^{-17} A/μm. Regarding contact scaling, interface engineering and optimized deposition processes have reduced the contact length to 20–40 nm, achieving a minimal contact pitch of 80 nm and a low specific contact resistivity. These developments highlight the strong potential of scaled a-IGZO TFTs. This article also summarizes and prospects their potential applications in monolithic 3-dimensional integration and high-density memory fields.

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1 Introduction

Since Gordon Moore proposed "Moore's Law" in the 20th century, the integrated circuit industry has developed and evolved around this core principle. As a fundamental law in the semiconductor field, Moore's Law posits that the number of transistors integrated per unit area on a chip doubles approximately every 18-24 months[1-4]. The essential driver of this trend is the continuous scaling of transistor dimensions. By constantly reducing critical device dimensions, integrated circuits have not only optimized manufacturing costs but also achieved leapfrog development in performance enhancement and integration density breakthroughs. However, as the channel length (L_{ch}) of traditional silicon-based transistors continues to scale below 10 nm, the influence of the drain-source voltage (V_{DS}) on the channel significantly increases. This leads to degraded gate control capability, resulting in a series of short-channel effects, including increased subthreshold swing (SS), drain-induced barrier lowering (DIBL), and elevated off-state current. Consequently, ensuring that the integrated circuit industry continues to follow "Moore's Law" in the post-Moore era has become a new challenge for the industry. The emergence of monolithic three-dimensional integration technology offers a new approach to overcoming the bottleneck of dimensional scaling. This technology vertically stacks transistors compatible with back-end-of-line (BEOL) processes onto transistors or device arrays fabricated using front-end processes[5]. While significantly increasing integration density, it also opens up new possibilities for diverse circuit function designs. In this context, thin film transistors (TFTs) demonstrate significant value due to their high cost-effectiveness, potential for large-scale manufacturing, and good compatibility with BEOL processes[6-12]. However, the carrier mobility of most current commercial TFT materials remains significantly lower than that of crystalline silicon[13-16]. Among various TFT technologies, oxide TFTs exhibit unique advantages. They not only inherit the process advantages of traditional amorphous silicon TFTs but also increase carrier mobility by an order of magnitude, significantly narrowing the performance gap with crystalline silicon. Additionally, they feature extremely low off-state current.

In recent years, with the rapid development of oxide TFTs in fields such as high-density storage and three-dimensional integration[17-27], requirements for their dimensions,

power consumption, integration density, and performance have become increasingly stringent[28]. In the field of dynamic random access memory (DRAM), traditional DRAM cells typically consist of one transistor and one separate capacitor. Since this capacitor often requires special processes to achieve high-density stacking, it is difficult to make such capacitors fully compatible with standard digital silicon-based complementary metal-oxide-semiconductor (CMOS) processes. Furthermore, it is challenging to achieve efficient integration with logic circuits across all process types and technology nodes. In this context, capacitor-less DRAM structures based on oxide TFTs have become a research hotspot. This structure requires only two transistors to achieve memory functionality. Oxide semiconductor materials, represented by amorphous indium-gallium-zinc oxide (a-IGZO), leverage their extremely low off-state leakage current caused by wide bandgaps. This allows oxide TFTs to serve simultaneously as read transistors and storage capacitors[29,30]. This innovative structure not only eliminates the need for separate capacitors, thereby providing substantial area savings, but is also fully compatible with mainstream digital CMOS technology[31-37]. However, to fully exploit the density and performance potential of this capacitor-less DRAM structure, higher requirements are imposed on the oxide TFT devices themselves. Currently, traditional large-size TFTs are inadequate for applications requiring high integration and high performance, failing to meet these demands. Therefore, advancing the dimensional scaling of oxide TFTs has become a key direction for technological breakthroughs. This measure can further increase integration density by reducing device dimensions and helps optimize core performance indicators such as switching speed, promoting the development of this technology to higher levels.

This review focuses on the dimensional scaling of oxide TFTs and systematically summarizes recent research progress in the field of a-IGZO TFT scaling. The content covers planar and vertical single-gate transistors, double-gate transistors, and transistor contact length (L_C) scaling technologies. Finally, we summarize the main challenges currently facing this field and provide an outlook on future development trends.

2 Channel Length Scaling of Single-Gate a-IGZO TFTs

In 2004, Hosono et al.[38,39] first proposed the a-IGZO material and successfully fabricated a-IGZO TFTs using it as the channel material. The Hall mobility of this TFT can reach approximately 10 $cm^2/(V\ s)$, which is an order of magnitude higher than that of traditional amorphous silicon (a-Si:H). As amorphous semiconductors, a-Si:H relies on covalent bonding, with carriers transported through sp^3 hybrid orbitals. Due to the strong directionality of sp^3 hybrid orbitals, changes in bond angles significantly affect electron energy levels. Additionally, the presence of high-density deep-level tail states

results in low carrier mobility. In contrast, the conduction band bottom of a-IGZO materials exhibits highly ionic characteristics. The ns orbitals of adjacent metals can directly overlap, and the orbital shape is isotropic, making it insensitive to changes in bond angles (as shown in Figure 1(a)). Therefore, its Hall mobility is similar to that of crystalline oxide semiconductors (as shown in Figure 1(b)), significantly outperforming covalently bonded amorphous semiconductors.

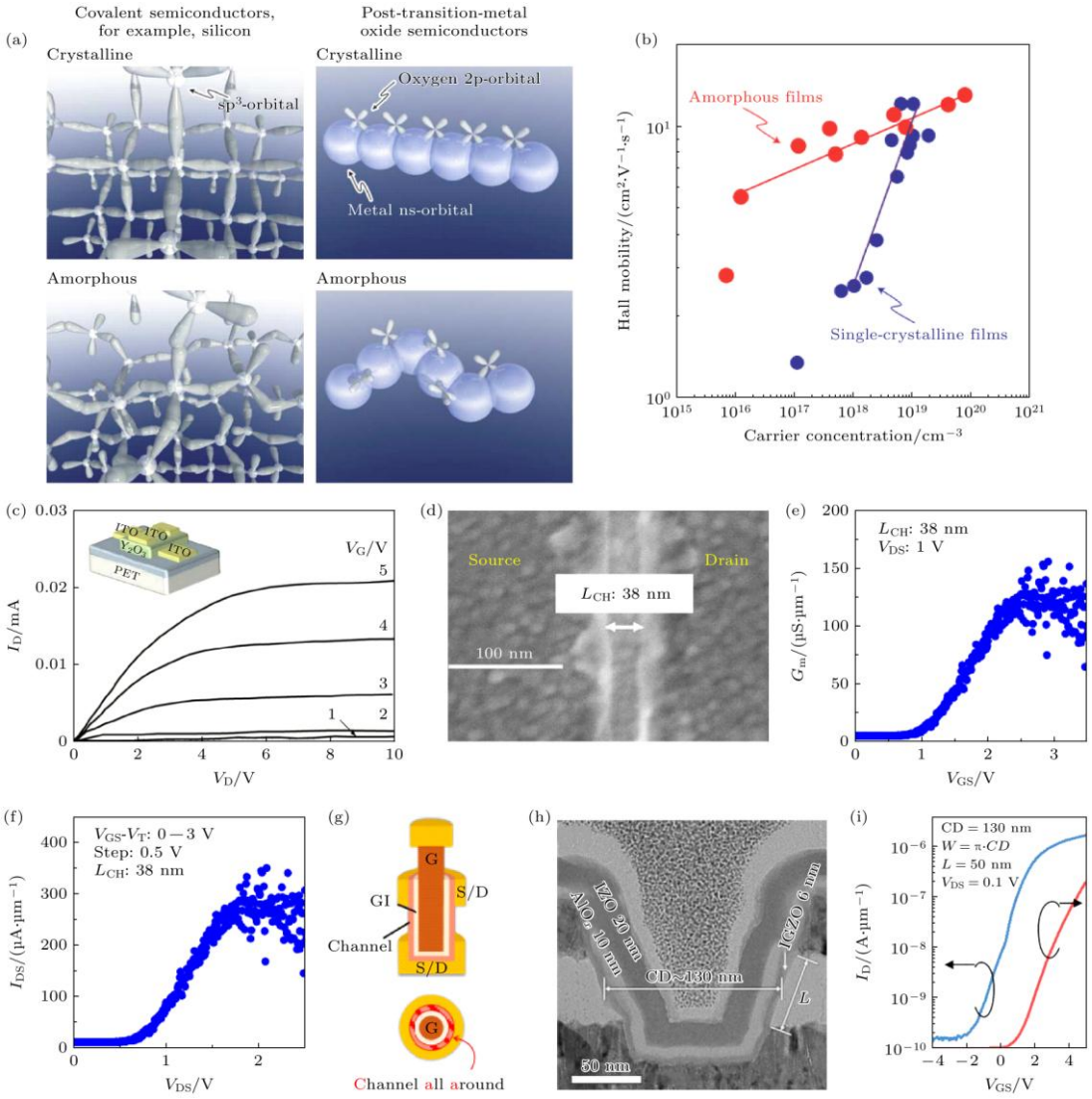

Fig. 1 (a) Electron cloud schematics of a-Si:H (left) and a-IGZO (right); (b) schematic of Hall mobility in crystalline and amorphous IGZO; (c) output curves of an a-IGZO transistor; (d) SEM image of an a-IGZO transistor; (e) transconductance curve of an IGZO transistor, with a maximum transconductance of 125 μS/μm @ V_{DS} = 1 V; (f) output curves of an a-IGZO transistor, with an on-current of 350 μA/μm @ (V_{GS} - V_T = 3.0 V, V_{DS} = 2.5 V); (g) schematic of a CAA-IGZO transistor; (h) cross-sectional TEM image of a CAA-IGZO transistor; (i) transfer curve of a CAA-IGZO transistor (CD = 50 nm) [39-41,45].

Since the introduction of amorphous indium gallium zinc oxide (a-IGZO) materials, their significant advantages have attracted sustained and widespread attention in both

academia and industry. This has prompted extensive research by numerous scientists and engineers. Currently, a-IGZO has achieved commercial application in fields such as flat-panel displays. It also demonstrates significant potential for application research in monolithic three-dimensional integration and novel memory technologies. To further expand its application in advanced integrated circuits and high-density integration systems, promoting the scaling of a-IGZO transistors to smaller dimensions has become a direct and critical technological development path. This approach is essential for enhancing integration density and system performance. Implementing this path is of great significance for overcoming existing technical bottlenecks and meeting the future demands of electronic devices for high integration and high performance.

As scaling technology continues to evolve, frontier exploration in scientific research has delved into the nanometer scale. For instance, at the 2020 Symposium on VLSI Technology and Circuits (VLSI), Samanta et al.[41] successfully demonstrated an a-IGZO thin-film transistor (TFT) with a channel length scaled down to 38 nm. This achievement marked significant progress in the field. The scanning electron microscope (SEM) image of this device is shown in Fig. 1(d), where the source and drain electrodes were patterned using electron-beam lithography. By scaling the channel length to 38 nm, the device achieved a maximum effective mobility of 34 $cm^2/(V\ s)$ at a carrier concentration of approximately 5×10^{12} cm^{-2}. The subthreshold swing (SS) was as low as 74.4 mV/decade. Furthermore, when the channel thickness was scaled from 6 nm to 3.6 nm, the device mobility showed no significant degradation. Meanwhile, the device achieved a maximum transconductance of 125 μS/μm at V_{DS} = 1 V (as shown in Fig. 1(e)). It also realized a high on-state current of 350 μA/μm at V_{GS}-V_T = 3.0 V and V_{DS} = 2.5 V. At V_{DS} values of 0.1 and 1 V, the SS values were 87 mV/decade and 210 mV/decade, respectively, with a drain-induced barrier lowering (DIBL) of 187 mV/V. The electrical characteristics of the device are illustrated in Fig. 1(e) and (f).

Compared with traditional planar TFTs, vertical TFTs feature smaller dimensions. Their core advantage lies in the "dimensional reconstruction" of the device structure. Unlike traditional planar structures, the source and drain of a vertical TFT are not coplanar. Instead, they are vertically separated by an isolation layer (insulating material). The channel is located between the source and drain and adheres to the vertical sidewall of the isolation layer. Conductive carriers flow in the vertical direction, fundamentally breaking through the dimensional limitations of lateral layouts. Since the first report of vertical TFTs, research and technical achievements in the field of short-channel vertical TFTs have significantly surpassed those of short-channel planar TFTs during the same period[42-44]. In 2021, Duan et al.[45] innovatively proposed a channel-all-around (CAA) vertical IGZO TFT (as shown in

Fig. 1(g)). The channel of this transistor is oriented vertically, surrounding the gate from all directions. This configuration effectively increases the channel width, thereby enabling the transistor to achieve superior charge control capabilities and electrical performance. Fig. 1(h) presents the cross-sectional transmission electron microscope (TEM) image of a device fabricated by this team, featuring a critical dimension of 130 nm and a channel length of 50 nm. The device exhibits an on-state current greater than 30 μA/μm and an extremely low off-state current below 1.8×10^{-17} A/μm (as shown in Fig. 1(i)).

3 Channel Length Scaling of Dual-Gate a-IGZO TFTs

The characteristic length λ of a transistor can be expressed by the formula $\lambda = \sqrt{t_b t_{ox}/\varepsilon_b \varepsilon_{ox}}$, where $\varphi(x)$ represents the potential distribution along the source-drain direction; t_b is the semiconductor thickness; t_{ox} is the gate oxide thickness; ε_b is the dielectric constant of the semiconductor; and ε_{ox} is the dielectric constant of the gate oxide. To significantly improve the electrical performance of a-IGZO transistors, an ultra-short channel length is an indispensable and decisive key factor. However, if the channel length is simply shortened without simultaneously scaling the characteristic length of the device, the fabricated devices will suffer from severe short-channel effects. These effects include DIBL, increased SS, and threshold voltage roll-off (V_t roll-off). Therefore, to realize an a-IGZO transistor with an ultra-short channel, it is necessary to minimize the characteristic length of the device as much as possible.

In long-channel devices, the distribution of defect states is relatively uniform. However, when the channel length is reduced to below 50 nm, the proportion of interface defect states in the total defect states increases significantly due to the substantial reduction in channel volume. Under the influence of a strong lateral electric field, defect states may exhibit a non-uniform distribution along the channel direction. Specifically, in the high-field region near the drain end, the defect activation energy decreases, leading to an increase in trap-assisted tunneling current. Meanwhile, the DIBL effect and threshold voltage roll-off further amplify the impact of defect states on the electrical performance of the device. In particular, deep-level traps act as recombination centers for carriers under high-voltage conditions, thereby exacerbating the degradation of subthreshold characteristics. Consequently, when the channel length of fabricated single-gate a-IGZO transistors is scaled to below 50 nm, significant short-channel effects can be clearly observed through electrical performance testing. This phenomenon indicates that as the channel length enters the nanoscale, the electrical characteristics of transistors are prominently affected by short-channel effects. This poses new challenges for the optimization and stable control of device performance.

To enhance the electrostatic control of the gate over the channel and suppress short-channel effects, the dual-gate structure has been widely introduced. The rationale for adopting a dual-gate structure is that, under the influence of two gates, electron accumulation in a-IGZO is no longer limited to the bottom surface. Instead, channels form simultaneously on both the top and bottom surfaces of the semiconductor. Due to the relatively thin semiconductor thickness, the top and bottom channels overlap, causing carriers to tend to accumulate in the overlapping region. This accumulation effect effectively reduces the impact of interface defects, roughness, and interface states on mobility, thereby increasing the on-state current of the device. Meanwhile, the dual-gate structure further enhances the electrostatic control capability of the gate, effectively reducing the subthreshold swing, DIBL, and off-state current of the transistor. Based on the three-dimensional Poisson equation $\frac{\mathrm{d}E_x}{\mathrm{d}_x}+\frac{\mathrm{d}E_y}{\mathrm{d}_y}+\frac{\mathrm{d}E_z}{\mathrm{d}_z}=-\frac{\rho}{\varepsilon}$, it can be seen that the left side of the equation represents the sum of electric field gradients. Under specific physical conditions, this can be considered a constant value. Therefore, enhancing the gate control capability of the top gate, back gate, or side gate of the channel will weaken the influence of the source-drain voltage on the channel. Through analysis and calculation of relevant physical models and boundary conditions, the characteristic length formula for dual-gate transistors can be derived as $\lambda_2 = t_{\mathrm{b}}t_{\mathrm{ox}}\varepsilon_{\mathrm{b}}/(2\varepsilon_{\mathrm{ox}})$. Compared with the characteristic length of single-gate transistors, the characteristic length of dual-gate transistors is $\sqrt{1/2}$ times that of the former. This mathematical result theoretically confirms that the dual-gate structure has significant advantages in transistor size scaling.

In 2022, Chen et al.[46] reported an ultra-thin dual-gate a-IGZO transistor with a channel length of 30 nm (as shown in Fig. 2(a)). By adopting the dual-gate structure, the minimum subthreshold swing of this transistor was only 63.4 mV/decade, close to the theoretical ideal value of 60 mV/decade. It also exhibited a low DIBL of 10 mV/V and a maximum transconductance of up to 559 μS/μm. Benefiting from the enhanced electrostatic control of the channel by the dual-gate structure, its transconductance and static on-state performance were superior to those of previously reported single-gate devices. The relevant electrical characteristics are shown in Fig. 2(b) and (c). To further break through the limits of device scaling and improve three-dimensional integration density, Liao et al.[47] proposed a novel vertical-channel dual-gate IGZO TFT structure in 2024 (as shown in Fig. 2(d)) and applied it to high-density DRAM cells. This device adopts a vertical structure with a channel length of 120 nm. Under coordinated dual-gate control, it demonstrated excellent electrical performance: it achieved a high on-state current of 45.5 μA/μm and an SS of 68 mV/decade at V_{GS} - V_{T} = 1.0 V and V_{DS} = 1 V (as shown in Fig. 2(e) and (f)). The above research results not

only verify that the vertical dual-gate structure possesses good gate control capabilities at the nanoscale but also demonstrate the considerable potential of this technology in promoting the development of integrated circuits toward higher integration density and achieving lower power consumption.

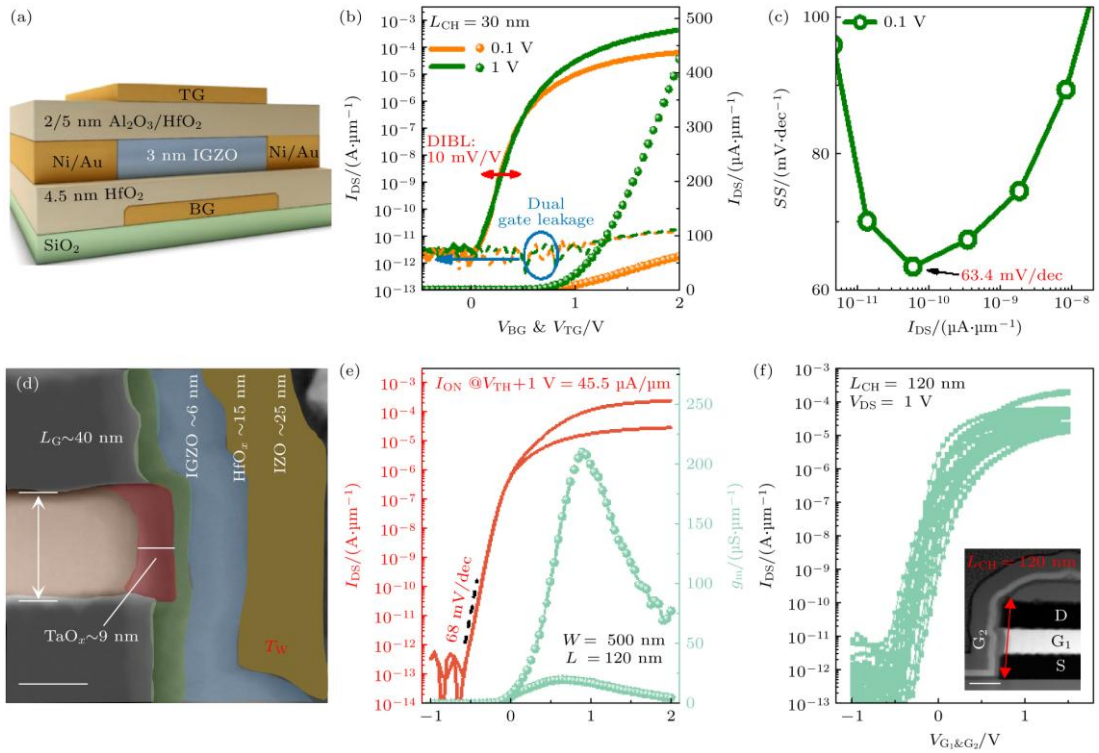

Fig. 2 (a) Schematic diagram of a dual-gate a-IGZO transistor structure; (b), (c) transfer characteristic curve and subthreshold swing of the dual-gate a-IGZO transistor (L_{ch} = 30 nm); (d) cross-sectional TEM image of a vertical dual-gate IGZO transistor; (e), (f) transfer characteristic curve and transconductance of the vertical dual-gate IGZO transistor, with an on-current of 45.5 μA/μm @ (V_{th} + 1) V (L_{ch} = 120 nm)[46,47].

4 Scaling of Contact Length in a-IGZO TFTs

In the overall transistor scaling, the contact pitch (CP) is a key parameter determining chip integration density. Its physical definition is the sum of the channel length (L_{ch}) and the contact length (L_C), as shown in Figure 3(a). Therefore, achieving fundamental scaling of transistor dimensions requires collaborative optimization and simultaneous reduction of both the channel length and the contact length.

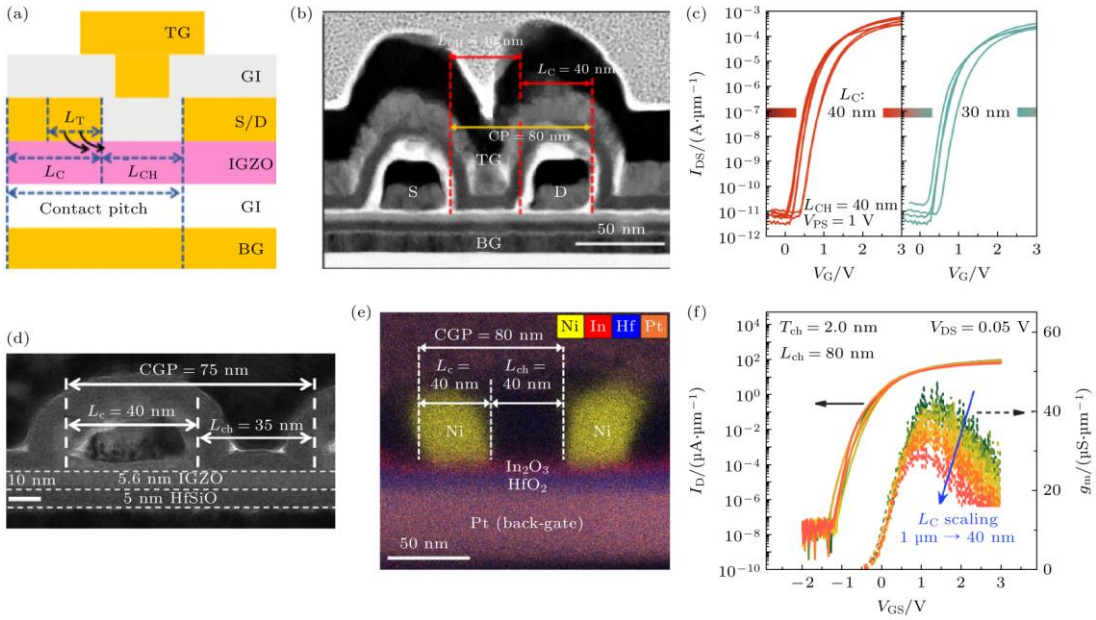

Fig. 3 (a) Schematic diagram defining contact pitch, contact length, and channel length; (b) cross-sectional TEM image of a short-channel device with a contact pitch of 80 nm; (c) transfer characteristic curves of devices when the contact length is scaled from 40 nm to 30 nm (L_{ch} = 40 nm); (d) cross-sectional TEM image of a high-performance dual-gate IGZO transistor; (e) cross-sectional TEM image of an ultra-scaled CGP indium oxide transistor; (f) transfer curves of transistors with L_{ch} = 80 nm and a channel thickness of 2 nm, as the contact length (L_C) is scaled from 1 μm to 40 nm [48-50].

Reducing the channel length enhances carrier transport efficiency and increases channel current density, thereby improving device switching speed and response characteristics. However, carrier transport in the contact region depends heavily on metal-semiconductor interface properties. As the contact length decreases, the effective contact area drops significantly, while interface scattering effects intensify. This leads to an exponential rise in contact resistance, which may degrade device performance and partially offset the benefits gained from channel scaling. Although amorphous indium gallium zinc oxide (a-IGZO) thin-film transistors (TFTs) have made significant progress in channel length scaling, with device dimensions moving from the micrometer scale to the tens of nanometers range, systematic solutions remain lacking for key issues such as contact length scaling, effective contact resistance control, and interface reliability maintenance. These challenges constitute critical bottlenecks restricting the development of oxide transistors toward higher integration density and superior comprehensive performance.

During the scaling of oxide TFTs, contact resistance has become increasingly prominent, serving as a key constraint on performance improvement. In recent years, research focus has shifted from channel structure optimization to precise regulation of contact interfaces. In 2024, Wu et al.[48] conducted an in-depth experimental study on

contact length scaling in dual-gate IGZO TFTs. By depositing source/drain metals under ultra-high vacuum conditions, they achieved a low specific contact resistance (R_n) of 340 Ω·μm and a specific contact resistivity (ρ_n) of 1.72×10^{-7} Ω·cm^2. Furthermore, by scaling the contact length (L_C) from 300 nm to 20 nm, they observed no significant degradation in long-channel device performance, whereas short-channel devices exhibited significant performance decline when L_C was less than 30 nm (as shown in Figure 3(c)). Ultimately, Wu et al.[48] fabricated high-performance short-channel devices with a contact pitch of 80 nm (where L_C is 40 nm and channel length L_{ch} is 40 nm), as illustrated in Figure 3(b). These devices achieved an ultra-high on-current of 68.4 μA/μm and a low subthreshold swing of 83.4 mV/decade.

To systematically investigate contact length scaling, optimize contact resistance, and fully leverage the high electrostatic control of dual-gate structures along with the passivation effect of oxygen ambient annealing, Zhao et al.[49] further studied single-gate and dual-gate IGZO TFTs. They examined device performance as the contact length scaled from 200 nm to 40 nm, ensuring high reliability and performance post-scaling. The results indicated that dual-gate IGZO transistors exhibited superior performance (as shown in Figure 3(d)). At room temperature, the devices achieved a low subthreshold swing of 60 mV/decade. Even when the temperature increased to 380 K, the devices maintained a low subthreshold swing of 76 mV/decade. With a channel length of 35 nm and a contact length of 80 nm, the transconductance exceeded 1 mS/μm, and the on-current reached 1.93 mA/μm. When the contact length was further scaled to 40 nm, device performance remained robust, with transconductance exceeding 0.75 mS/μm and on-current exceeding 1.33 mA/μm.

Significant progress has also been made in contact scaling within broader oxide semiconductor systems. Lin et al.[50] investigated the scaling characteristics of contact length and contact gate pitch (CGP = L_{ch}+L_C) in ultra-thin indium oxide field-effect transistors (as shown in Figure 3(e)). The team found that increasing the indium oxide channel thickness from 1.2 nm to 2 nm allowed them to modulate the Schottky barrier height at the metal/indium oxide interface via quantum confinement effects, causing a transition from positive to negative. This transition reduced the transfer length significantly from 76 nm to 36 nm. Based on this optimization, the fabricated transistors achieved the lowest contact resistance among oxide field-effect-transistors of 140 Ω·μm and a maximum drain current ($I_{D,\ max}$) of 1.57 mA/μm under an ultra-scaled CGP of 80 nm (as shown in Figure 3(f)). This achievement provides critical support for back-end-of-line compatible monolithic three-dimensional integration technology.

5 Conclusion and Outlook

Oxide TFTs have become an important research direction for post-Moore integrated circuits due to their excellent electrical properties, low-temperature fabrication processes, and good compatibility with back-end-of-line (BEOL) processes. Particularly as traditional silicon-based CMOS devices face constraints from short-channel effects and slowing scaling trends, a-IGZO TFTs demonstrate immense application potential in monolithic three-dimensional integration and high-density memory. This is attributed to their high carrier mobility despite their amorphous structure, low off-state current, and favorable interface characteristics. This review systematically summarizes research progress in the scaling of a-IGZO TFTs, covering key areas such as single-gate devices, dual-gate devices, and contact length scaling.

In the field of monolithic three-dimensional integration, stacking multiple device layers vertically significantly enhances chip integration density and functional diversity. Structurally, vertical channel TFTs (such as those with a channel-all-around architecture) overcome the physical scaling limitations of planar layouts via "dimensional reconstruction." This enables further reduction of channel length (to below 50 nm) while maintaining excellent gate control and electrical performance. The introduction of dual-gate structures further enhances electrostatic control over the channel, effectively suppressing short-channel effects. Consequently, a-IGZO TFTs can achieve near-ideal subthreshold swing (63.4 mV/decade) and low drain-induced barrier lowering (10 mV/V) even at a channel length of 30 nm. These structural innovations and process optimizations provide key technical support for the development of a-IGZO TFTs in three-dimensional integration. Regarding contact scaling, contact resistance has become a critical factor affecting performance as device dimensions shrink. By optimizing the metal/semiconductor interface and employing ultra-high vacuum deposition processes, contact resistance can be reduced to as low as 340 Ω·μm, with contact length scalable to 20-40 nm and contact pitch reaching 80 nm. In high-density memory applications, particularly in dynamic random-access memory (DRAM), a-IGZO TFTs are widely used in capacitor-less DRAM structures due to their extremely low off-state current (below 10^{-17} A/μm). This structure requires only two transistors for storage functionality, with the a-IGZO TFT serving both read and storage roles, thereby eliminating the need for independent capacitors and significantly increasing memory density.

Despite significant progress in the scaling of a-IGZO TFTs, several challenges remain. When the channel length falls below 30 nm, the negative effects of interface defect states intensify significantly, leading to subthreshold characteristic degradation and increased leakage current, which severely impacts device stability. As contact length

continues to shrink, contact resistance rises exponentially. Furthermore, interface thermal stability and electromigration reliability face severe tests, becoming key constraints on further device scaling. Additionally, for memory structures such as capacitor-less DRAM, data retention time and read/write endurance require further improvement to meet the demands of practical memory applications.

Looking ahead, scaling technology for a-IGZO TFTs will continue to advance in key directions. On one hand, researchers are actively exploring novel transistor structures such as gate-all-around (GAA) and nanosheet configurations. Optimizing these designs will further enhance gate control, effectively suppress short-channel effects, and improve device performance. On the other hand, by combining circuit design with architectural innovation, the performance advantages of a-IGZO TFTs in three-dimensional integration and memory systems can be fully leveraged. This will promote their application and development in high-density, high-performance memory and three-dimensional integration fields.

References

[1] Davari B, Dennard R H, Shahidi G G 1995 *Proceed. IEEE* **83** 595

[2] Dennard R H, Gaensslen F H, Yu H-N, Rideout V L, Bassous E, Leblanc A R 1999 *Proceed. IEEE* **87** 668

[3] Moore G E 2006 *IEEE Solid-St. Circ. Soc. Newsletter* **11** 37

[4] Jing W, Lundstrom M *Digest. International Electron Devices Meeting* San Francisco, CA, USA, December 8–11, 2002 p707

[5] Liu M G, Li Z, Lu W D, Chen K F, Niu J B, Liao F X, Wu Z J, Lu C Y, Li W Z, Geng D, Lu N D, Dou C M, Yang G H, Li L, Liu M *2024 IEEE Symposium on VLSI Technology and Circuits （VLSI Technology and Circuits）* Honolulu, HI, USA, June 16–20, 2024 p1

[6] Weber L F 2006 *IEEE Trans. Plasma Sci.* **34** 268

[7] Li W W, Geng D, Yang G H, Lu N D, Li L 2024 *IEEE Open J. Immers. Displays* **1** 51

[8] Yan S Z, Cong Z R, Lu N D, Yue J S, Luo Q 2023 *Sci. China Inf. Sci.* **66** 200404

[9] Lan L F, Zhang P, Peng J B 2016 *Acta Phys. Sin.* **65** 128504

[10] Li S S, Liang C X, Wang X X, Li T H, Song S M, Xin Y Q, Yang T L 2013 *Acta Phys. Sin.* **62** 077302

[11] Li Y, Zhu L, Chen C S, Zhu Y, Wan C J, Wan Q 2022 *Chin. Phys. Lett.* **39** 118501

[12] Liu Y, Wang L, Cai S T, Chen Y Y, Chen R, Xiong X M, Geng K W 2018 *Chin. Phys. Lett.* **35** 098502

[13] Kuo Y 2004 *Thin Film Transistors: Materials and Processes* （Vol. 1） （New

York: Springer） pp176–195

[14] Kamiya T, Nomura K, Hosono H 2010 *Sci. Technol. Adv. Mater.* **11** 044305

[15] Jang J, Oh J Y, Kim S K, Choi Y J, Yoon S Y, Kim C O 1998 *Nature* **395** 481

[16] Kimura M, Yudasaka I, Kanbe S, Kobayashi H, Kiguchi H, Seki S I, Miyashita S, Shimoda T, Ozawa T, Kitawada K 1999 *IEEE Trans. Electron Devices* **46** 2282

[17] Mo Y G, Kim M, Kang C K, Jeong J H, Park Y S, Choi C G, Kim H D, Kim S S 2011 *J. Soc. Inf. Display* **19** 16

[18] Chen J, Liu C T 2013 *IEEE Access* **1** 150

[19] Sugimoto A, Ochi H, Fujimura S, Yoshida A, Miyadera T, Tsuchida M 2004 *IEEE J. Sel. Top. Quant.* **10** 107

[20] Burrows P E, Graff G L, Gross M E, Martin P M, Shi M K, Hall M, Mast E, Bonham C, Bennett W, Sullivan M B 2001 *Displays* **22** 65

[21] Kina O, Matsubara R, Ito Y, Ishizaki M, Ito M 2011 *J. Imag. Soc. Jpn.* **50** 128

[22] Suzuki K, Yutani K, Nakashima M, Onodera A, Mizukami S, Kato M, Tano T, Tomono H, Yanagisawa M, Kamyama K 2011 *J. Imag. Soc. Jpn.* **50** 142

[23] Belmonte A, Oh H, Subhechha S, Rassoul N, Hody H, Dekkers H, Delhougne R, Ricotti L, Banerjee K, Chasin A, Setten M J v, Puliyalil H, Pak M, Teugels L, Tsvetanova D, Vandersmissen K, Kundu S, Heijlen J, Batuk D, Geypen J, Goux L, Kar G S *2021 IEEE International Electron Devices Meeting （IEDM）* San Francisco, CA, USA, December 11–16, 2021 p10.6.1

[24] Duan X L, Huang K L, Feng J X, Niu J B, Qin H B, Yin S H, Jiao G F, Leonelli D, Zhao X X, Jing W L, Wang Z G, Chen Q, Chuai X C, Lu C Y, Wang W W, Yang G H, Geng D, Li L, Liu M *2021 IEEE International Electron Devices Meeting （IEDM）* San Francisco, CA, USA, December 11–16, 2021 p10.5.1

[25] Chen C K, Duan X L, Yang G H, Lu C Y, Geng D, Li L, Liu M *2022 International Electron Devices Meeting （IEDM）* San Francisco, CA, USA, December 3–7, 2022 p26.5.1

[26] Lu W D, Zhu Z Y, Chen K F, Liu M G, Kang B M, Duan X L, Niu J B, Liao F X, Dan W, Wu X S, Son J, Xiao D Y, Wang G L, Yoo A, Cao K Y, Geng D, Lu N D, Yang G H, Zhao C, Li L, Liu M *2022 International Electron Devices Meeting （IEDM）* San Francisco, CA, USA, December 3–7, 2022 p26.4.1

[27] Tang W J, Liu J L, Sun C, Zheng Z J, Liu Y P, Yang H Z, Jiang C, Ni K, Gong X, Li X 2023 *IEEE Trans. Circuits I* **70** 5166

[28] Mukhopadhyaya K, Srividya P 2022 *Mater. Today Proceed.* **55** 414

[29] Luk W K, Dennard R H 2005 *IEEE J. Solid-St. Circ.* **40** 884

[30] Somasekhar D, Ye Y, Aseron P, Lu S-L, Khellah M M, Howard J, Ruhl G, Karnik T, Borkar S, De V K 2008 *IEEE J. Solid-St. Circ.* **44** 174

[31] Meinerzhagen P, Teman A, Giterman R, Edri N, Burg A, Fish A 2018 *Gain-cell Embedded DRAMs for Low-Power VLSI Systems-on-Chip*（Springer） pp13–46

[32] Garzón E, Greenblatt Y, Harel O, Lanuzza M, Teman A 2021 *IEEE Trans. VLSI Syst.* **29** 1319

[33] Bonetti A, Golman R, Giterman R, Teman A, Burg A 2020 *IEEE Trans. VLSI Syst.* **28** 646

[34] Chun K C, Jain P, Kim T-H, Kim C H 2011 *IEEE J. Solid-St. Circ.* **47** 547

[35] Kim W, Kih J, Kim G, Jung S, Ahn G 1994 *IEEE J. Solid-St. Circ.* **29** 978

[36] Giterman R, Bonetti A, Bravo E V, Noy T, Teman A, Burg A 2020 *IEEE Trans. Circuits I* **67** 1207

[37] Chun K C, Jain P, Lee J H, Kim C H 2011 *IEEE J. Solid-State Circ.* **46** 1495

[38] Hosono H 2018 *Nat. Electron.* **1** 428

[39] Nomura K, Ohta H, Takagi A, Kamiya T, Hirano M, Hosono H 2004 *Nature* **432** 488

[40] Fortunato E, Barquinha P, Martins R 2012 *Adv. Mater.* **24** 2945

[41] Samanta S, Han K Z, Sun C, Wang C K, Thean A V Y, Gong X *2020 IEEE Symposium on VLSI Technology* Honolulu, HI, USA, June 16–19, 2020 p1

[42] Hwang C-S, Park S-H K, Oh H, Ryu M-K, Cho K-I, Yoon S-M 2014 *IEEE Electron Device Lett.* **35** 360

[43] Ahn H-M, Moon S-H, Kwon Y-H, Seong N-J, Choi K-J, Hwang C-S, Yang J-H, Kim Y-H, Yoon S-M 2022 *IEEE Electron Device Lett.* **43** 1909

[44] Baek Y J, Kang I H, Hwang S H, Han Y L, Kang M S, Kang S J, Kim S G, Woo J G, Yu E S, Bae B S 2022 *Sci. Rep.* **12** 3094

[45] Duan X L, Huang K L, Feng J X, Niu J B, Qin H B, Yin S H, Jiao G F, Leonelli D, Zhao X X, Wang Z G, Jing W L, Wang Z B, Wu Y, Xu J, Chen Q, Chuai X, Lu C Y, Wang W W, Yang G H, Geng D, Li L, Liu M 2022 *IEEE Trans. Electron Devices* **69** 2196

[46] Chen K F, Niu J B, Yang G H, Liu M G, Lu W D, Liao F X, Huang K L, Duan X L, Lu C Y, Wang J W, Wang L F, Li M M, Geng D, Zhao C, Wang G L, Lu N D, Li L, Liu M *2022 IEEE Symposium on VLSI Technology and Circuits*（*VLSI Technology and Circuits*） Honolulu, HI, USA, June 12–17, 2022 p298

[47] Liao F X, Zhu Z Y, Chen K F, Yang G H, Liu M G, Lu W D, Wu Z J, Niu J B, Lu C Y, Kang B M, Shi J, Wu X S, Yu R S, Zhang W D, Zhang J, Wang G L, Yue J S, Wang J W, Wang L F, Geng D, Lu N D, Zhao C, Nathan A, Li L, Liu M *2024 IEEE International Electron Devices Meeting*（*IEDM*）San Francisco, CA, USA, December 7–11, 2024 p1

[48] Wu Z J, Niu J B, Lu C Y, Bai Z H, Chen K F, Wu Z H, Lu W D, Liu M G, Liao F

X, Geng D, Lu N D, Yang G H 2024 *IEEE Electron Device Lett.* **45** 408

[49] Zhao W J, Zhu S W, Li Q J, Hu Q L, Liu H G, Tong A Y, Zeng M, Huang R, Wu Y Q *2024 IEEE International Electron Devices Meeting（IEDM）*San Francisco, CA, USA, December 7–11, 2024 p1

[50] Lin J Y, Niu C, Lin Z H, Liu C, Lu J J, Wang H Y, Ye P D *2025 Symposium on VLSI Technology and Circuits （VLSI Technology and Circuits）* Kyoto, Japan, June 8–12, 2025 p1